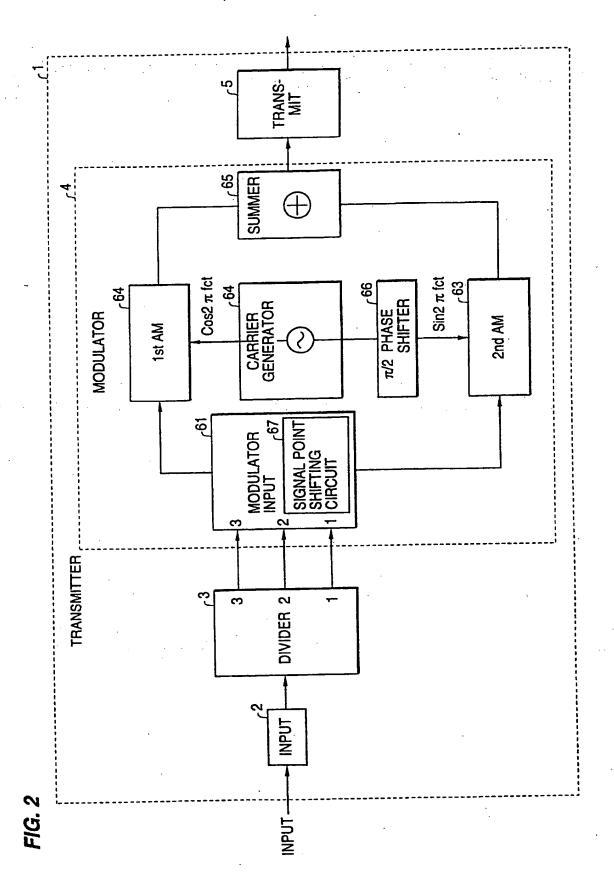
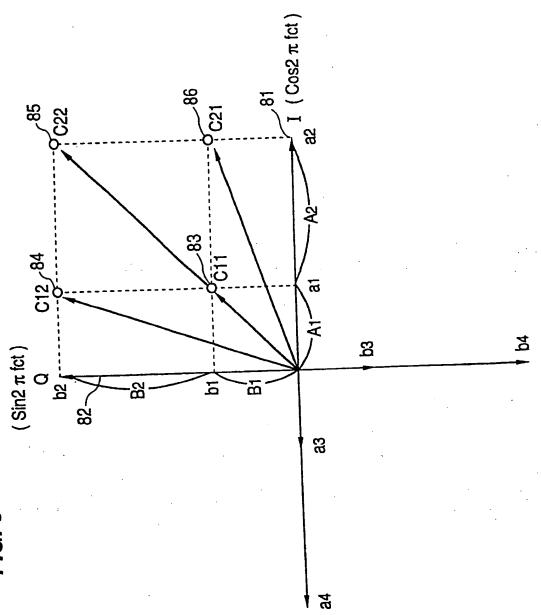
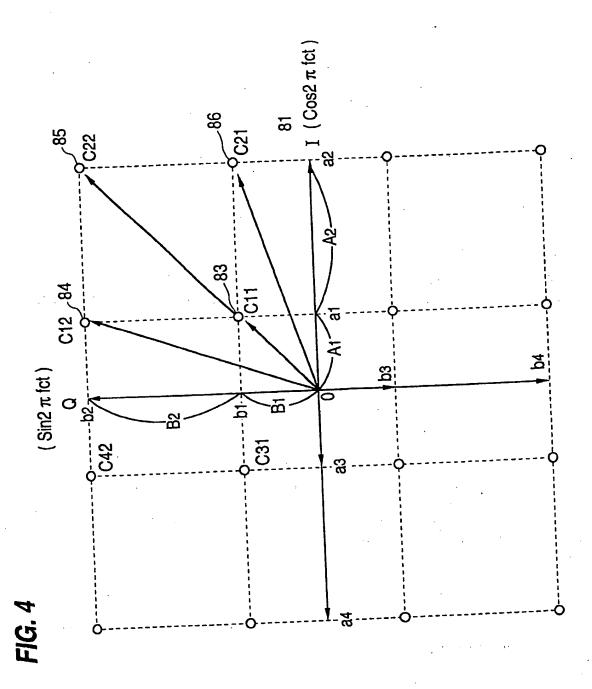
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FIG. 1





-1G. 3



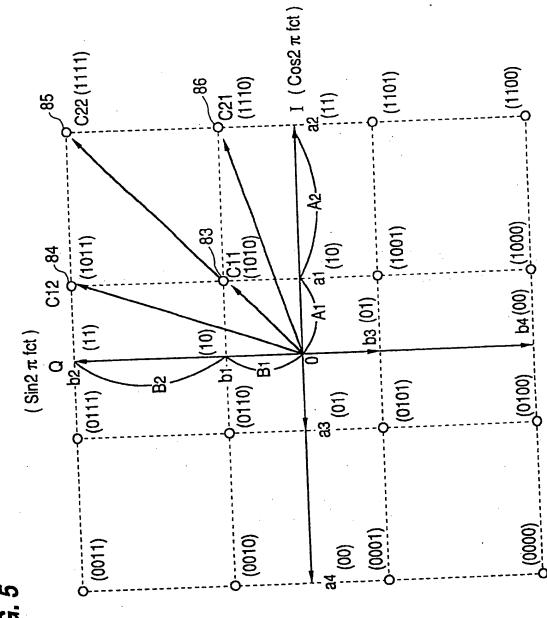


FIG. 5

FIG. 6

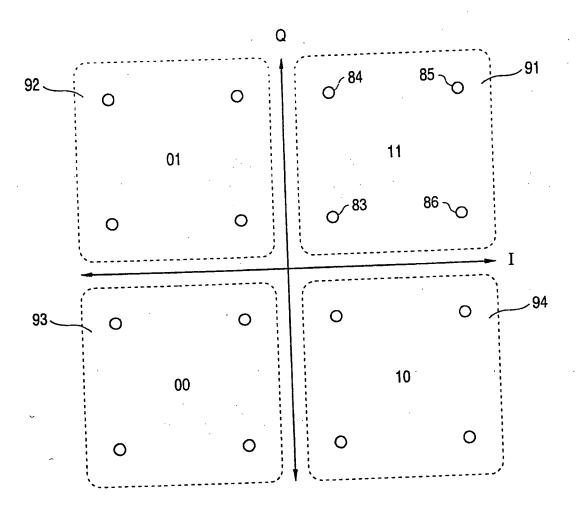


FIG. 7

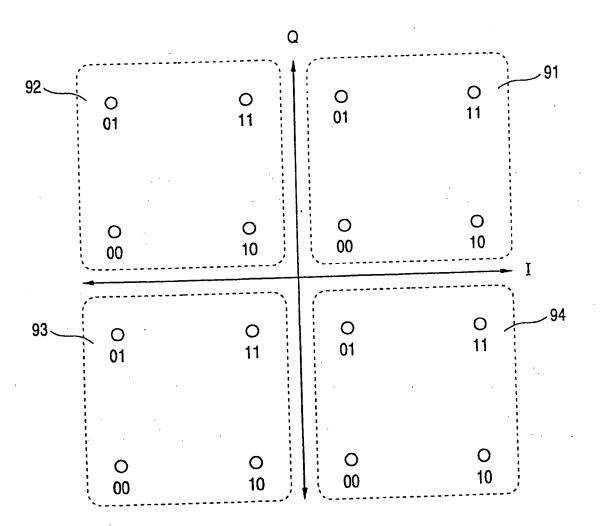
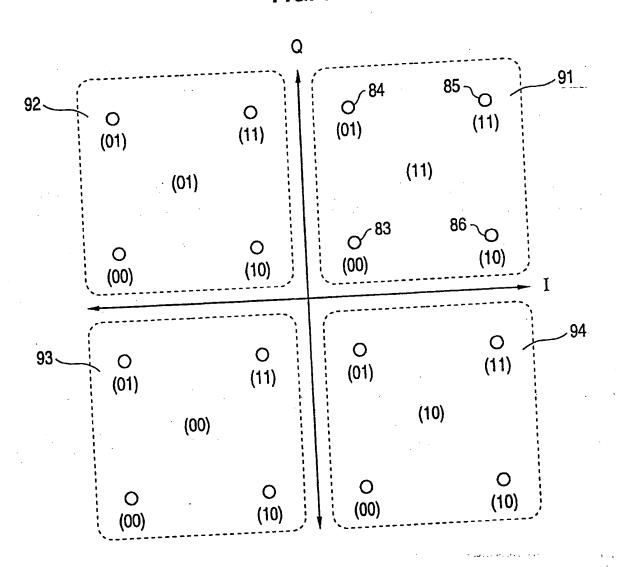
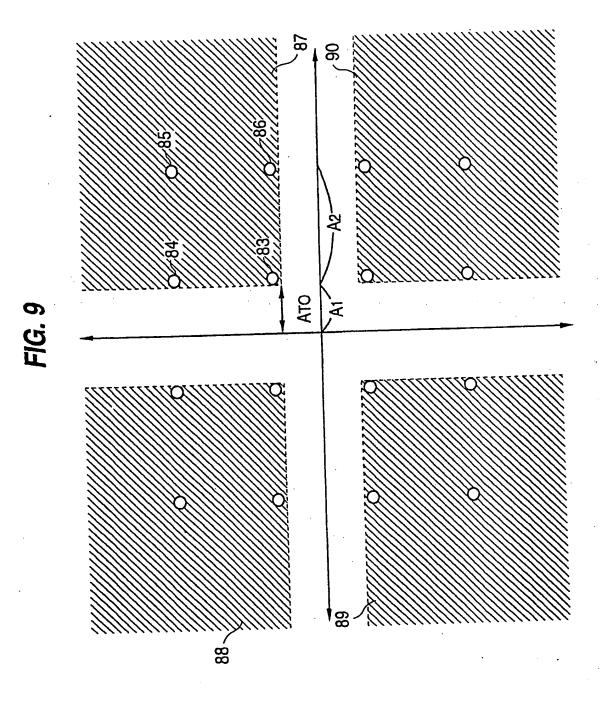
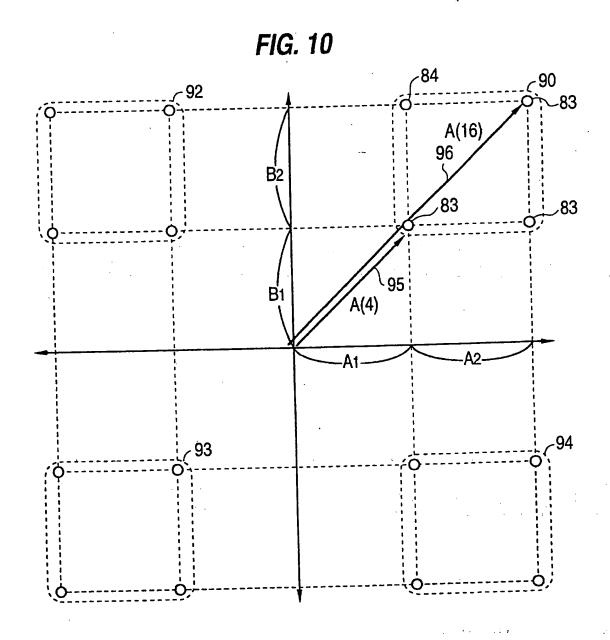


FIG. 8





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U.S. Patent

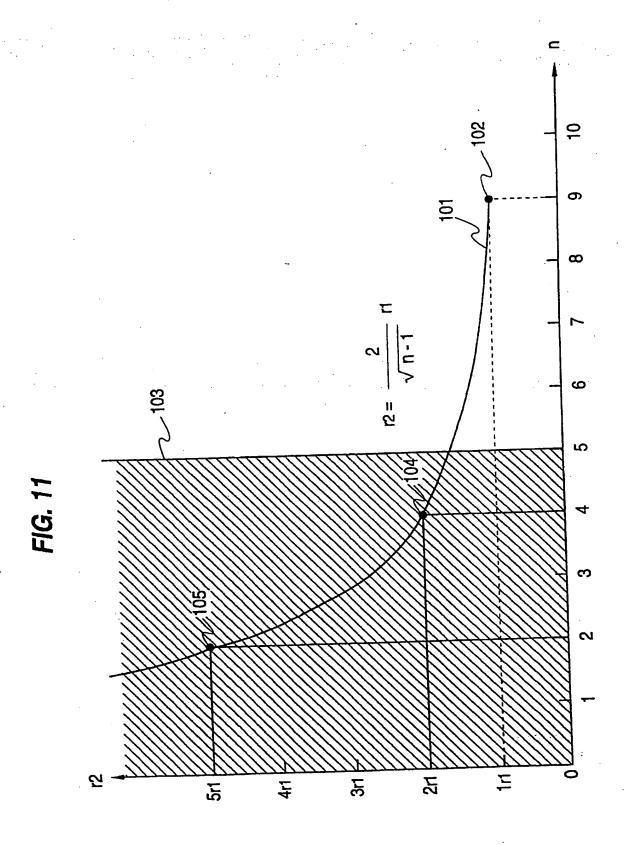
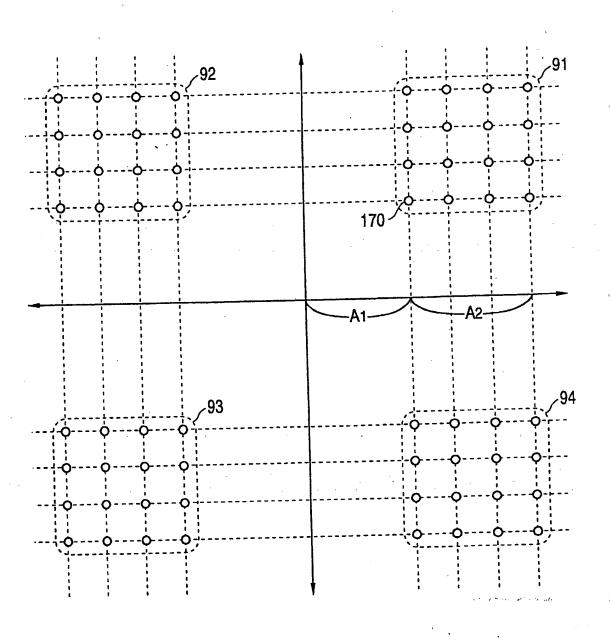
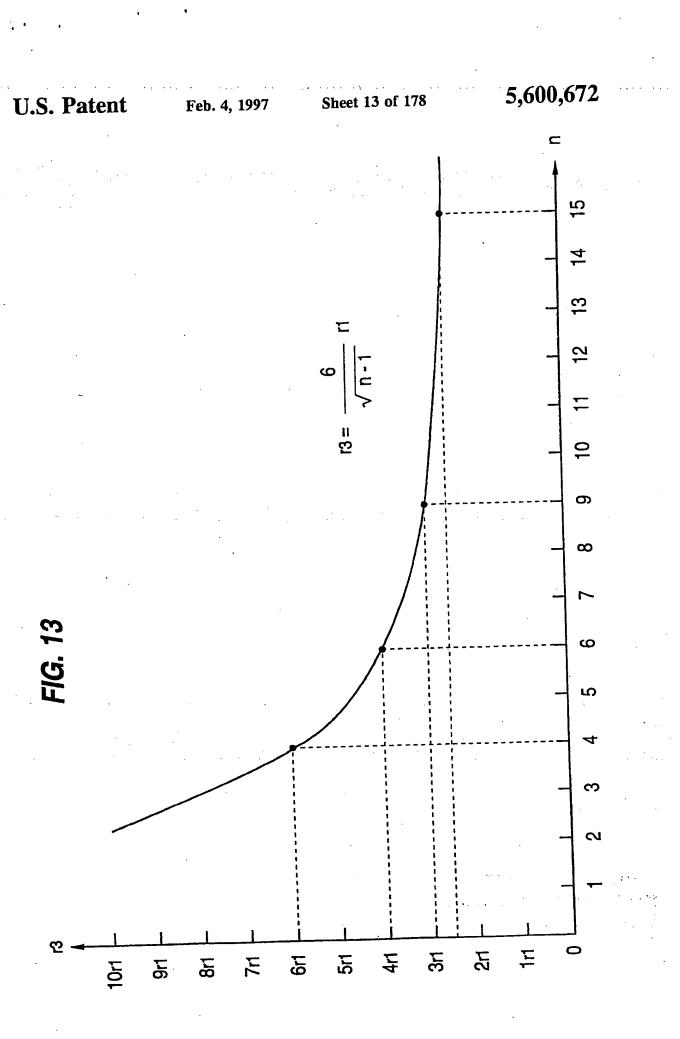
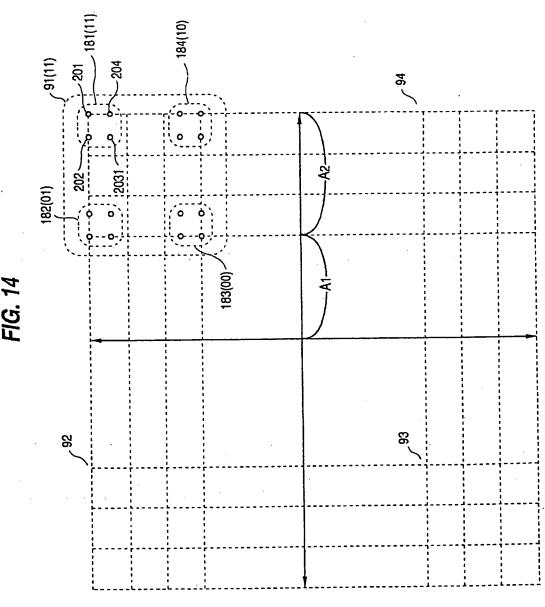


FIG. 12



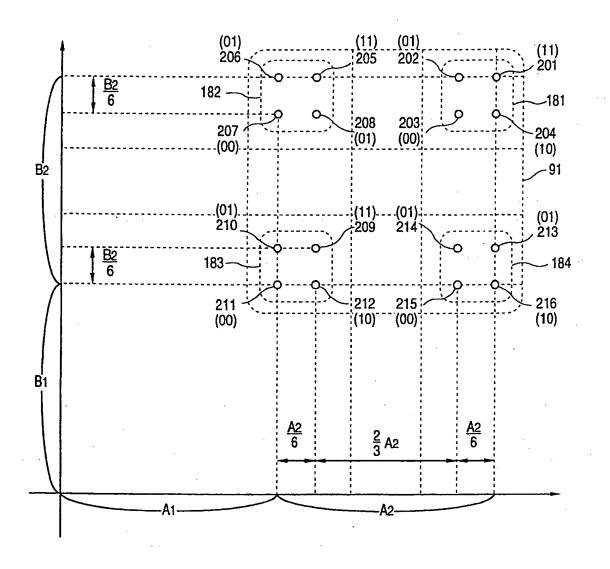


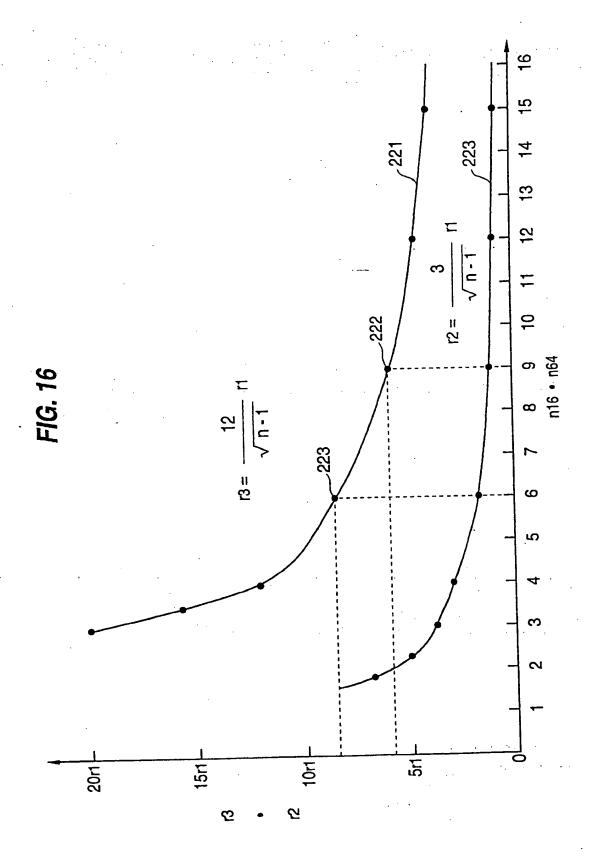


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FIG. 15

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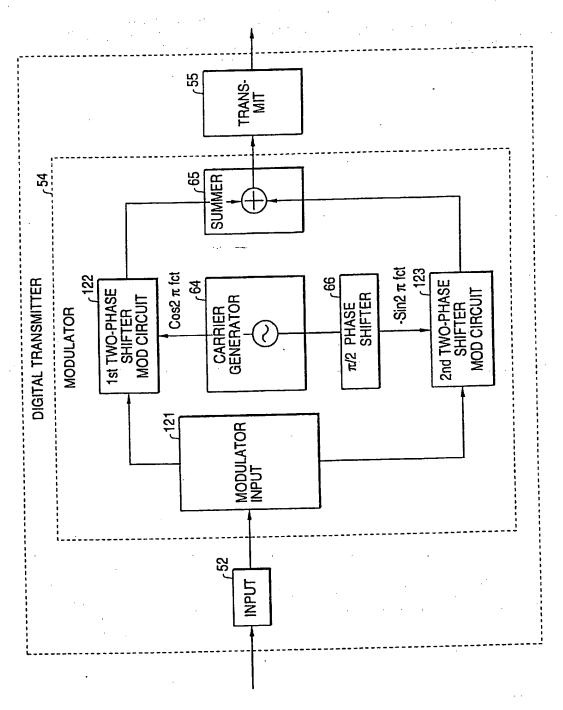
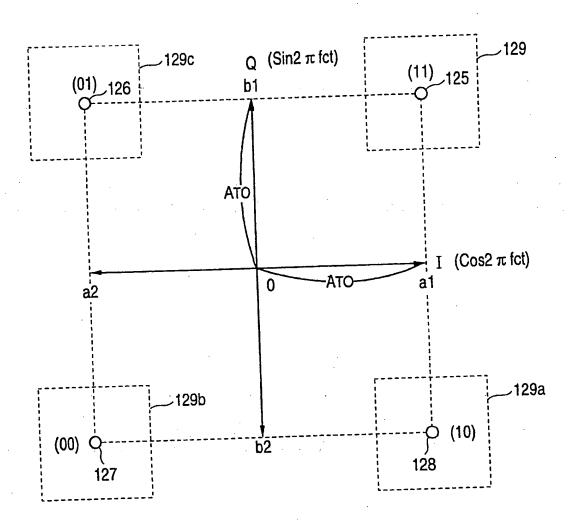
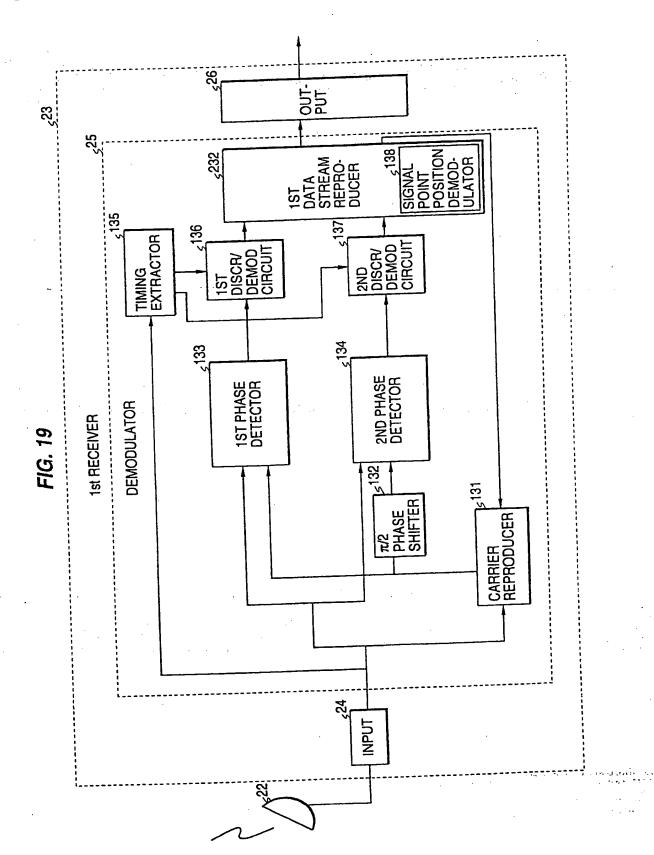
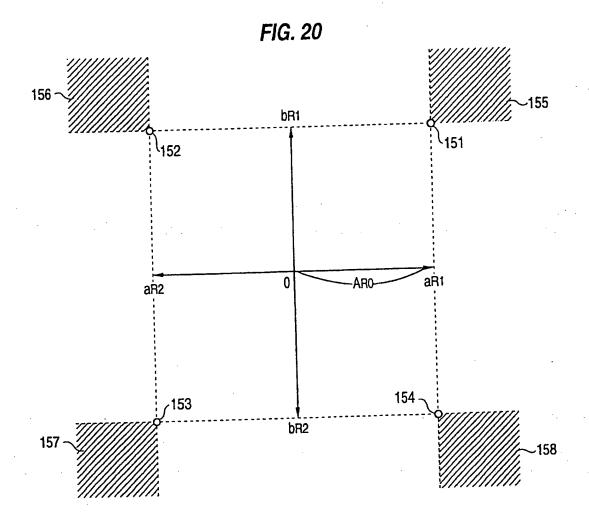


FIG. 17

FIG. 18







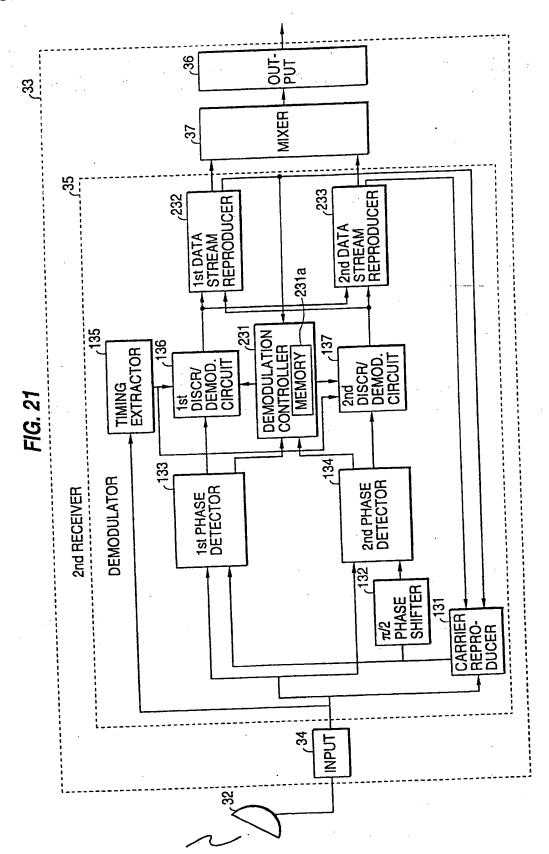
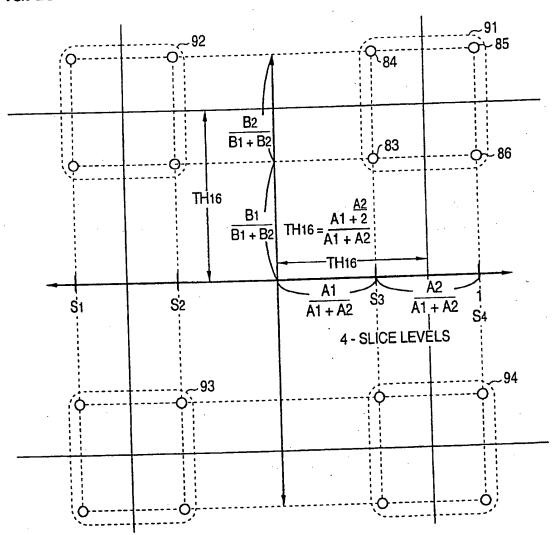


FIG. 22



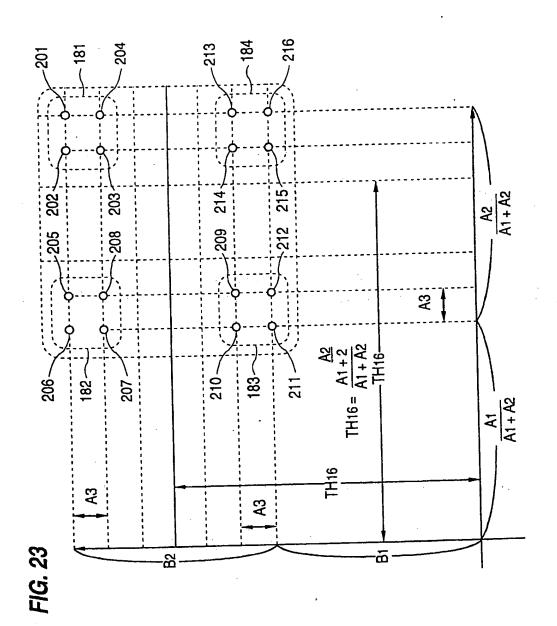
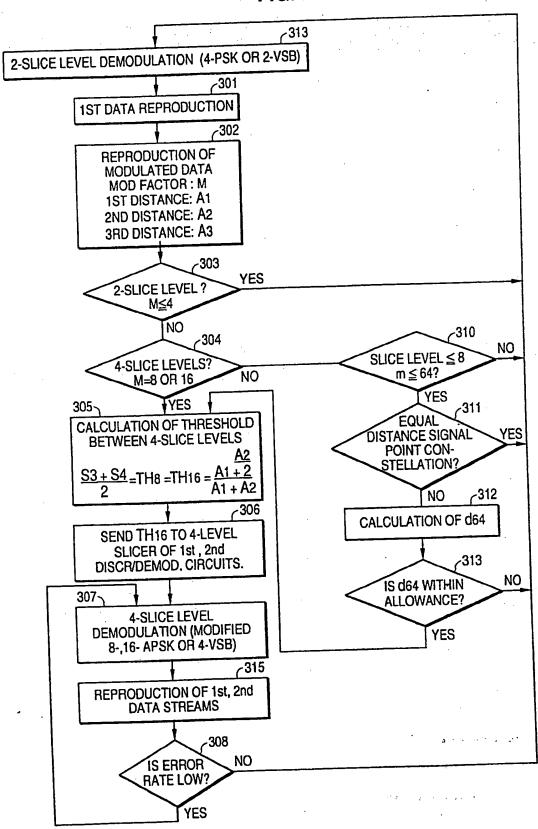
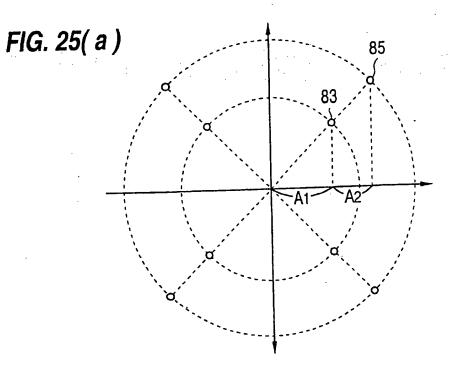
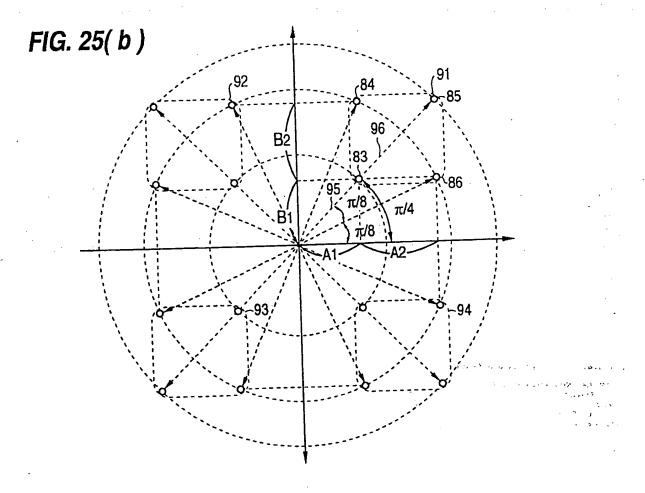
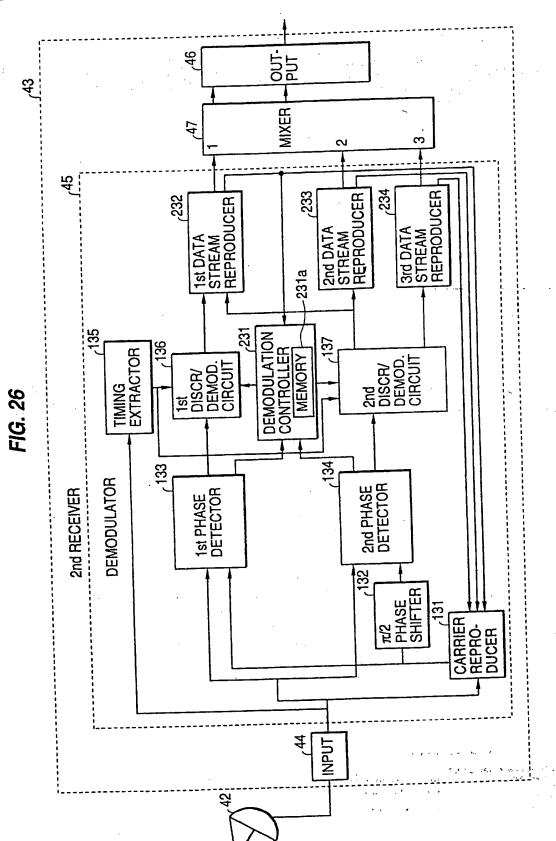


FIG. 24



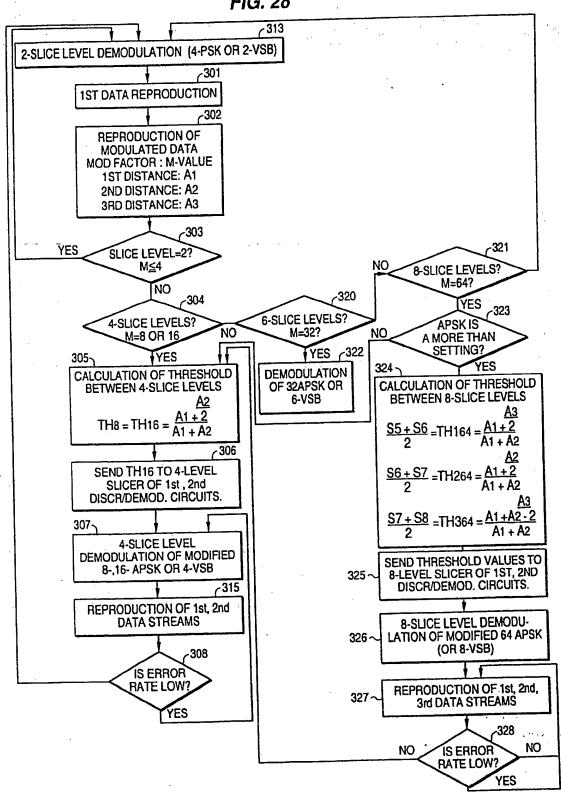


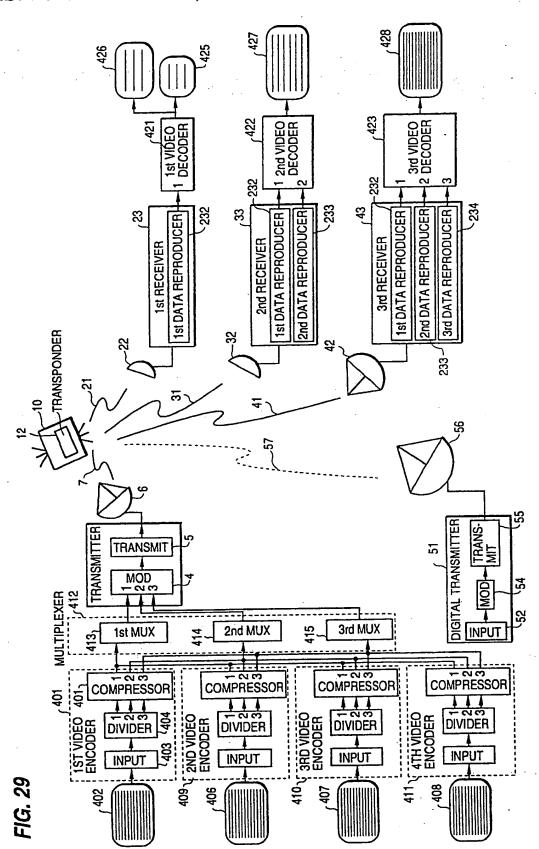


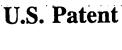


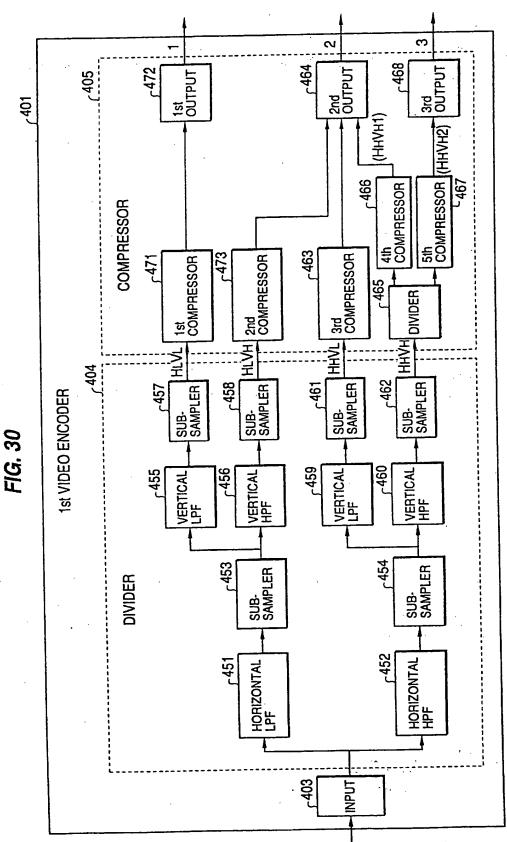
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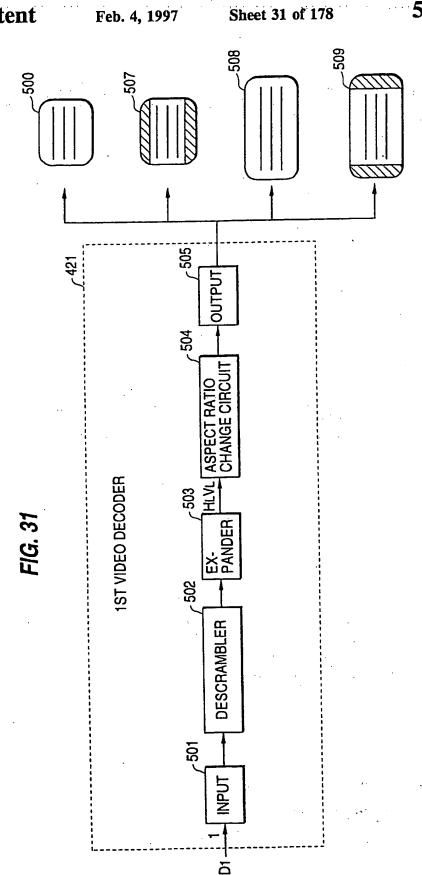
FIG. 28

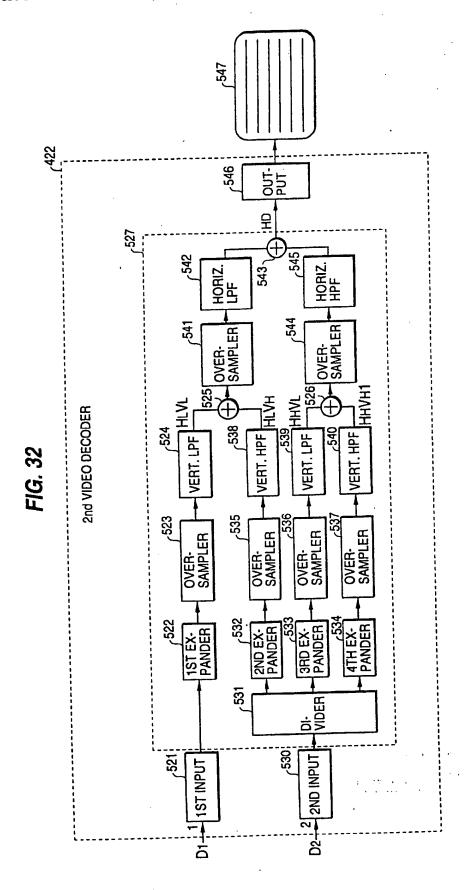


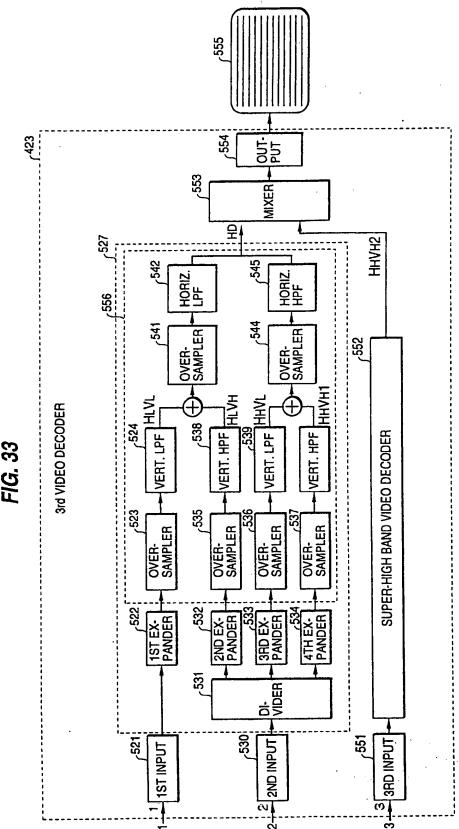


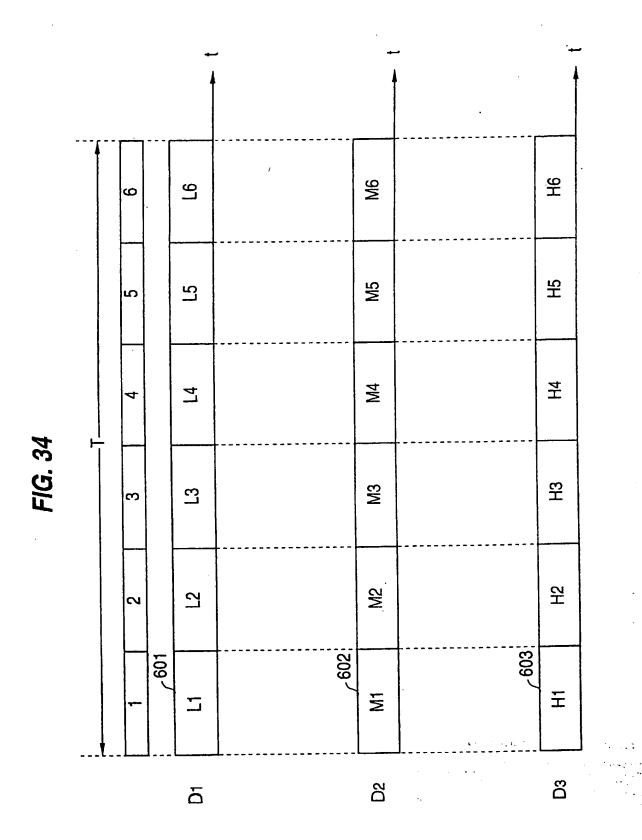


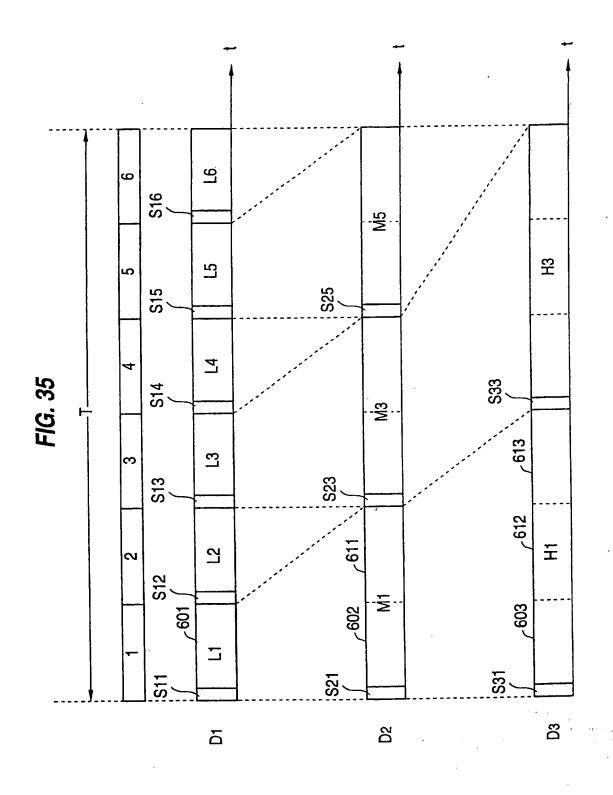




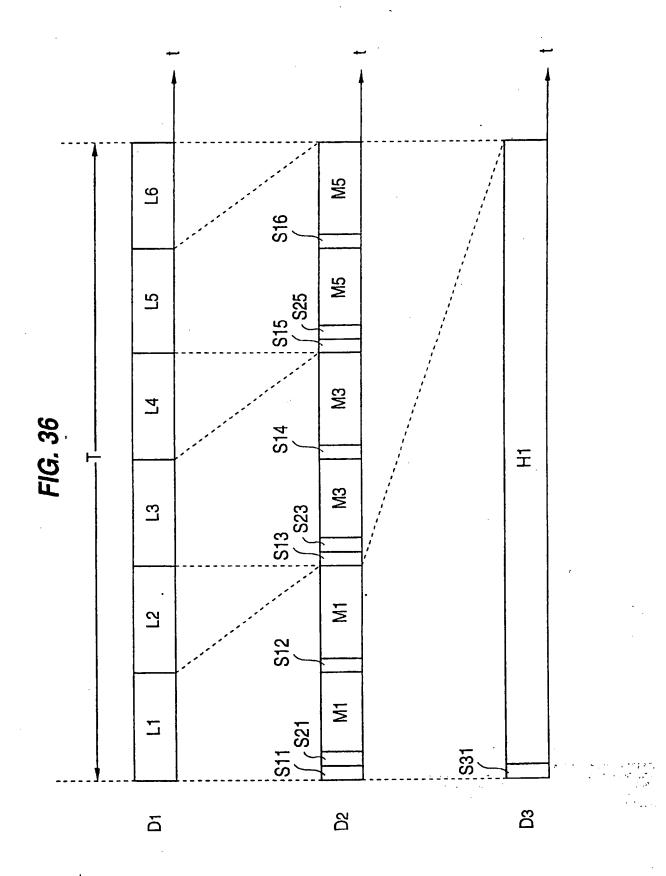


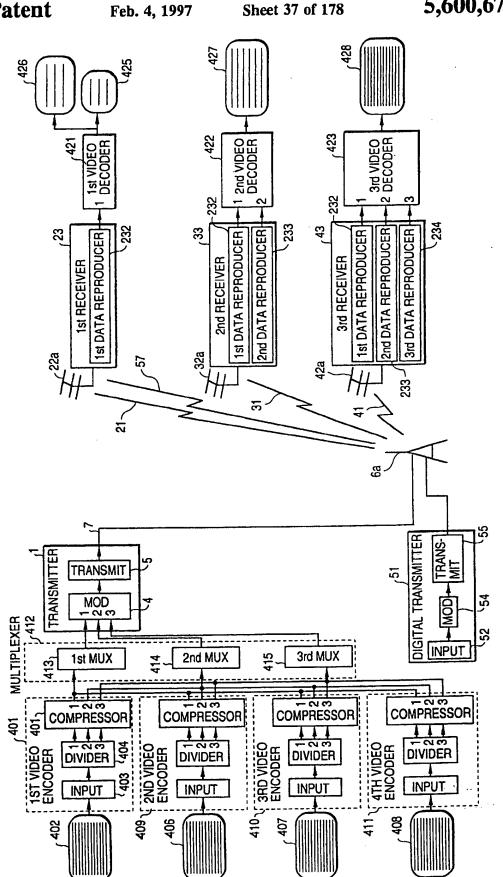


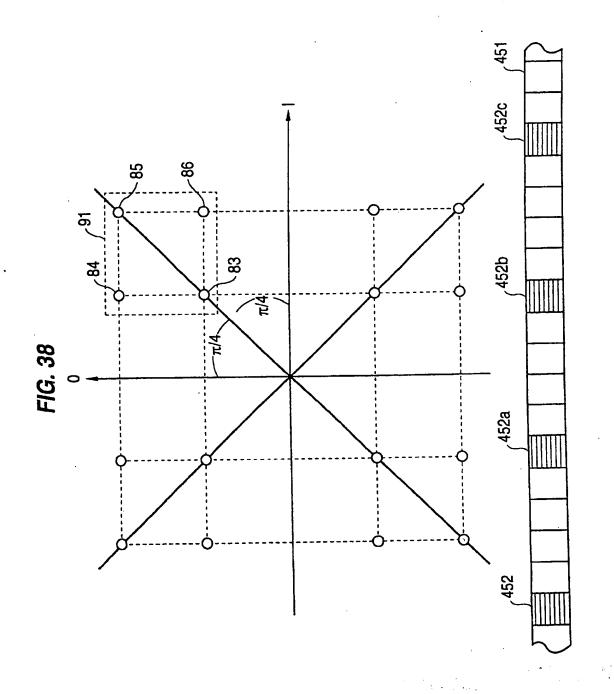


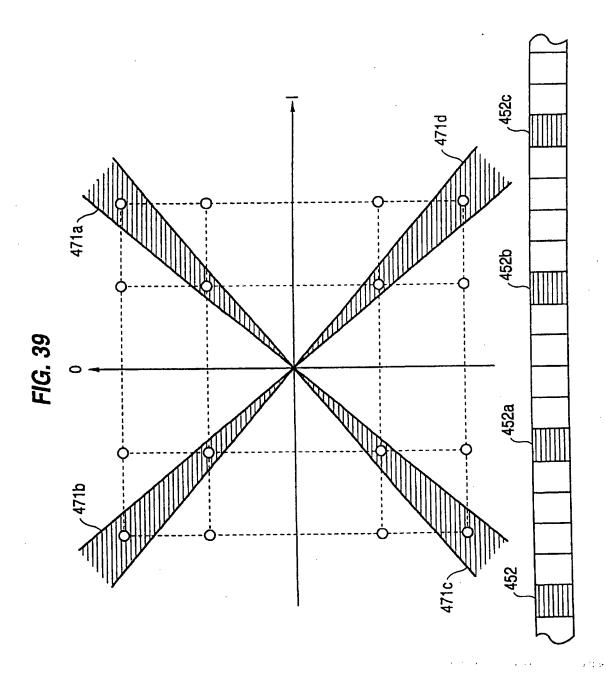


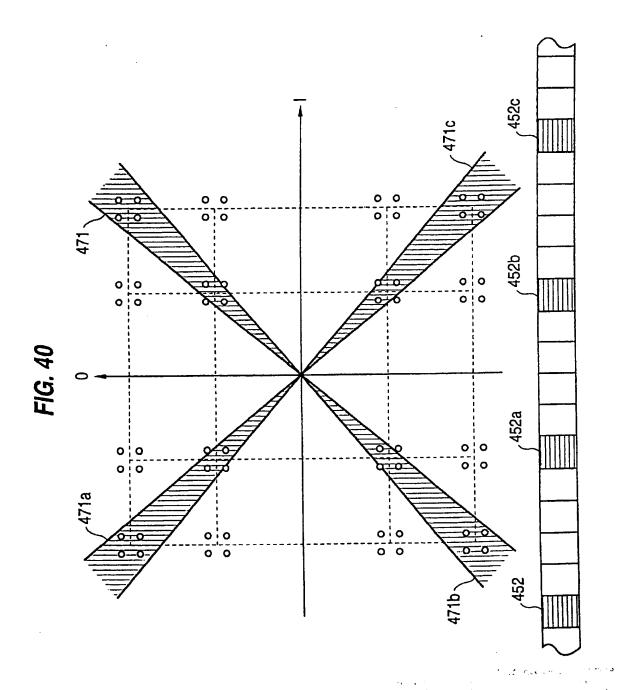
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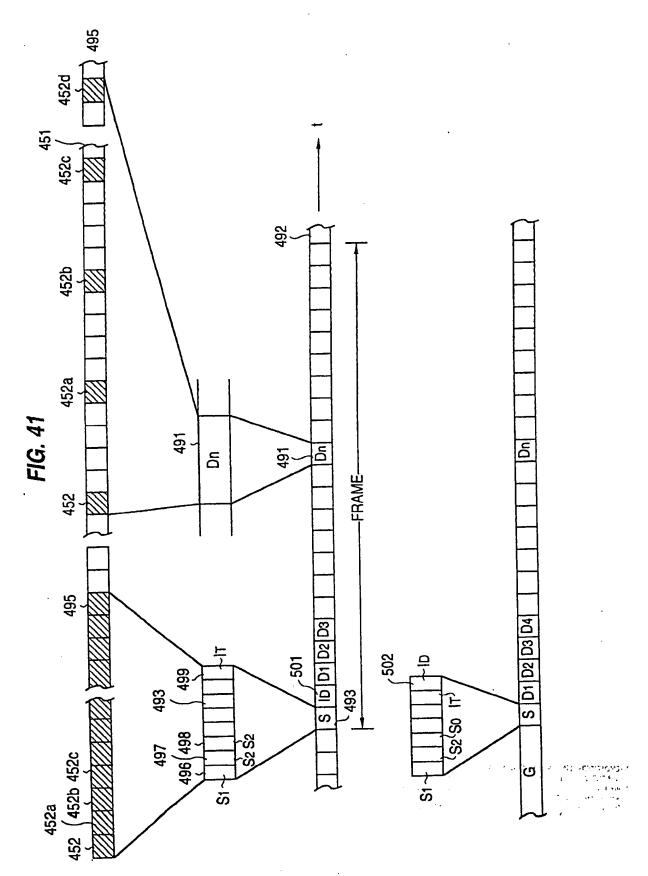


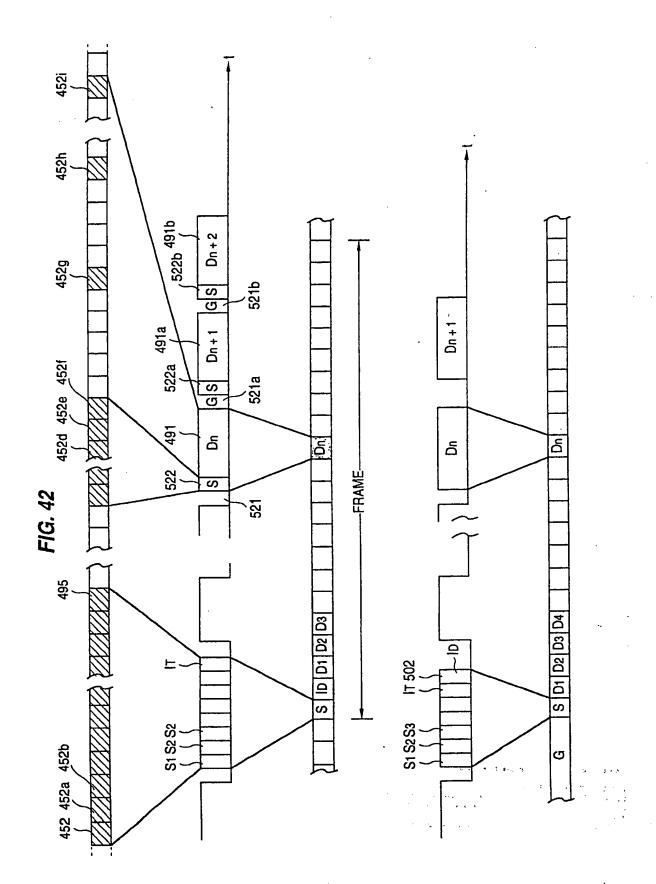


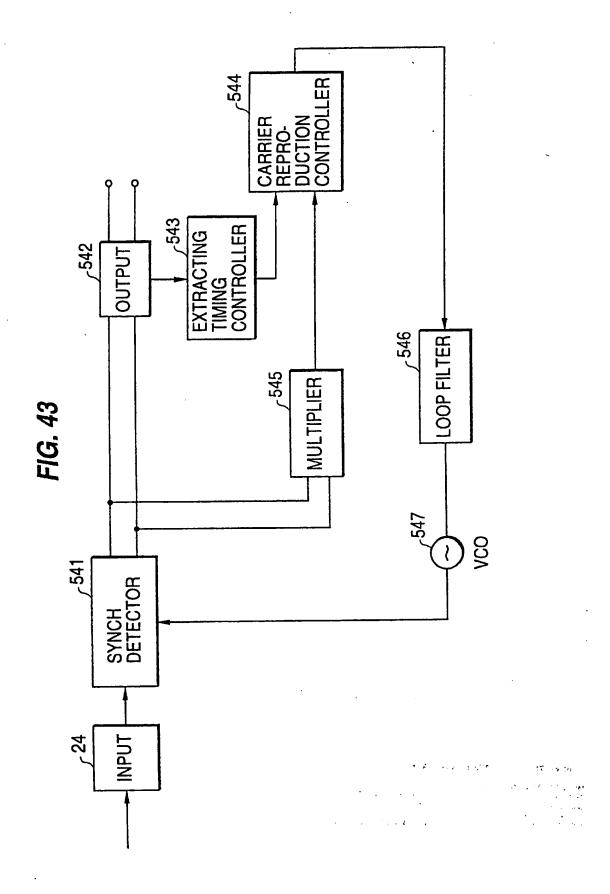


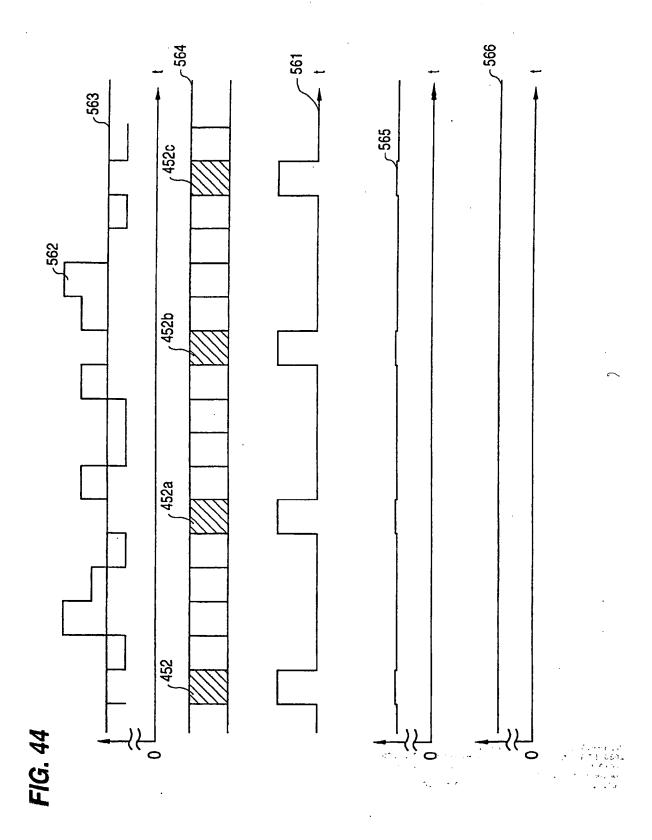


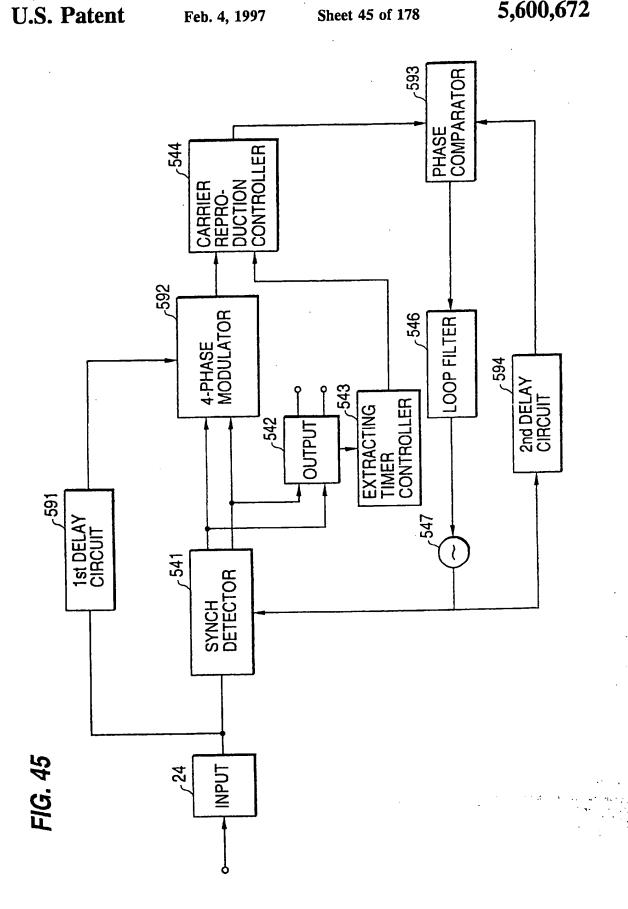


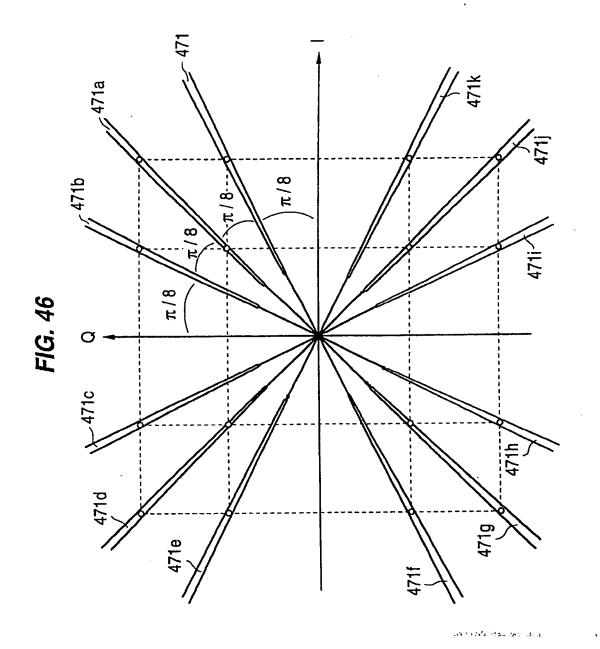


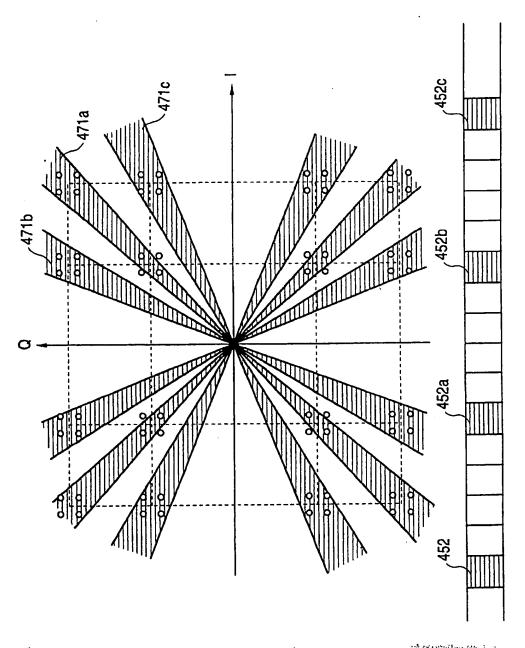












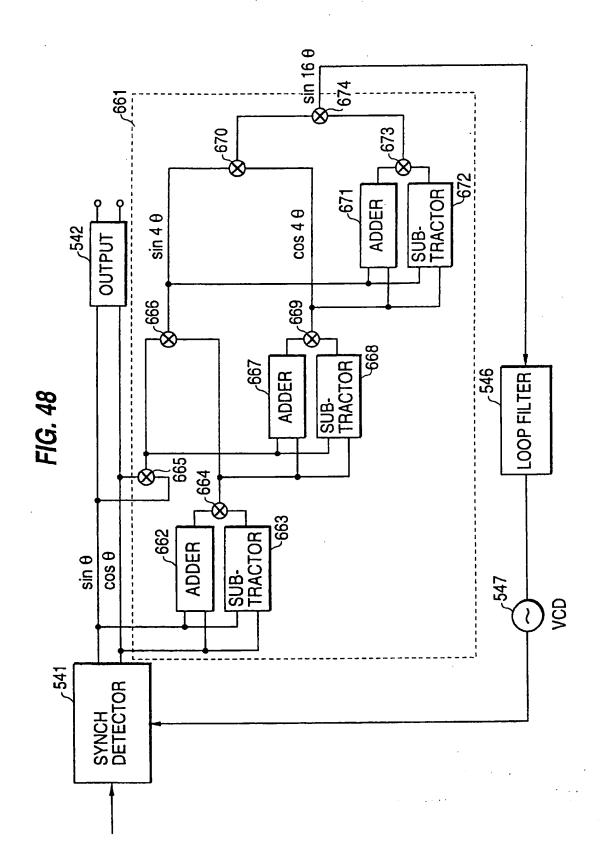
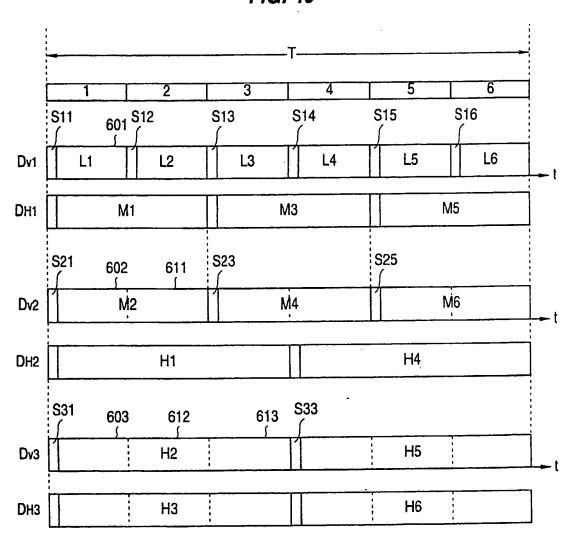
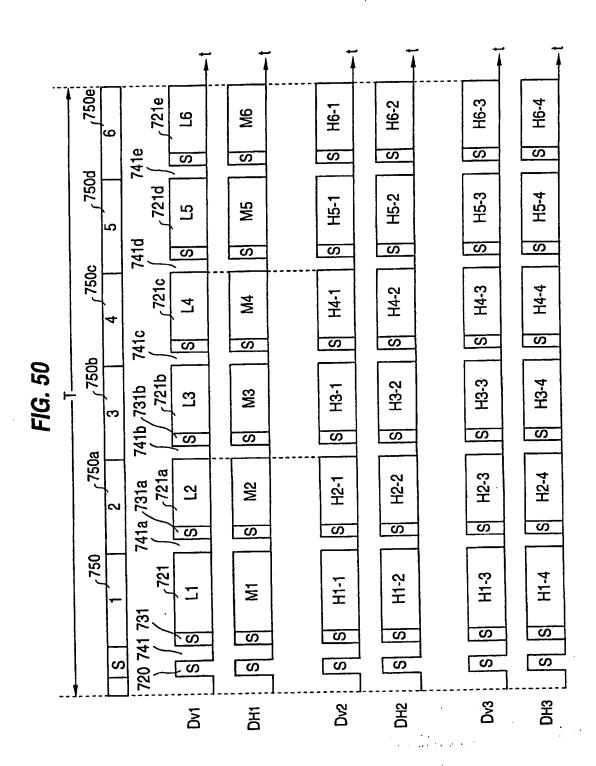


FIG. 49

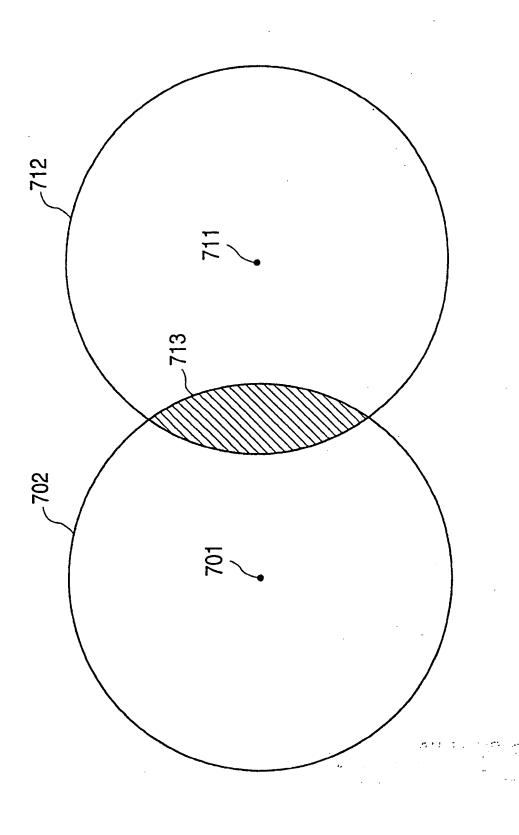


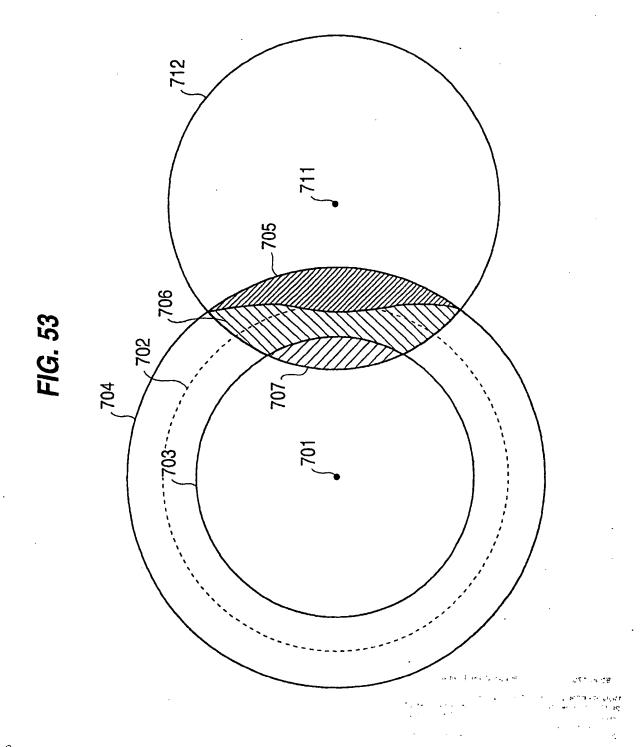


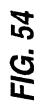
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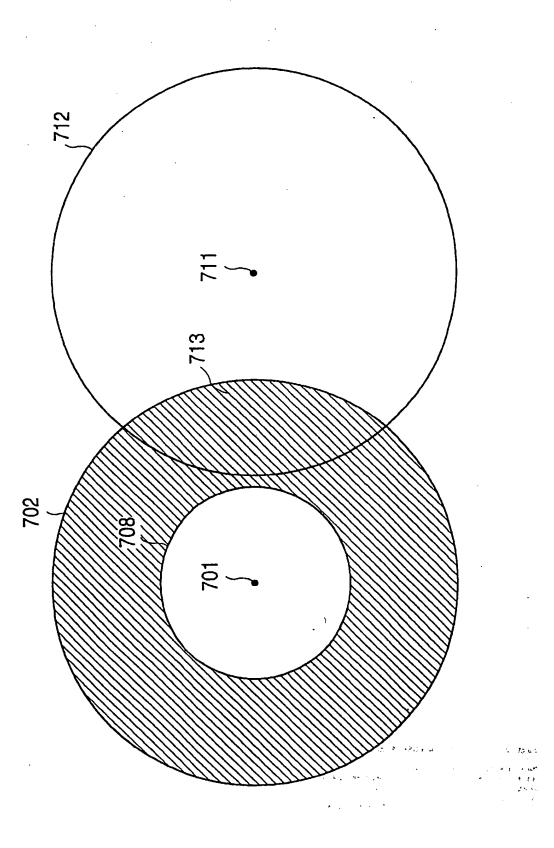
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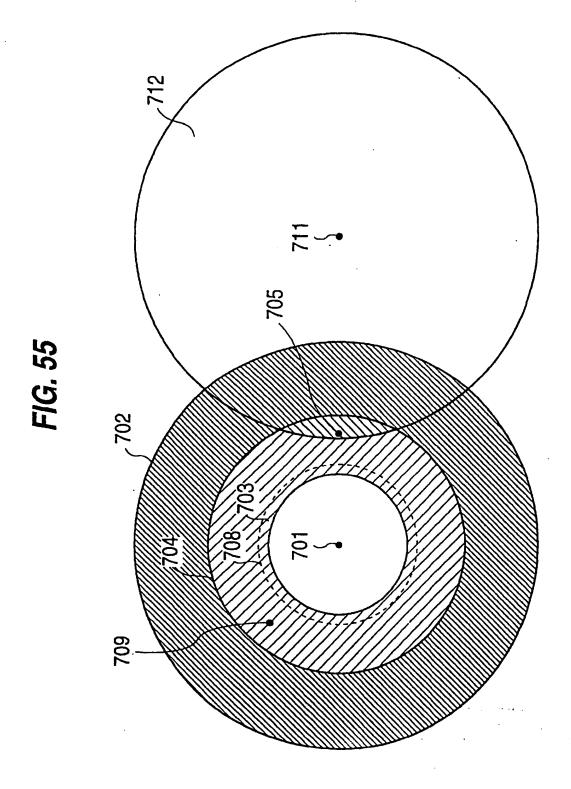
FIG. 52











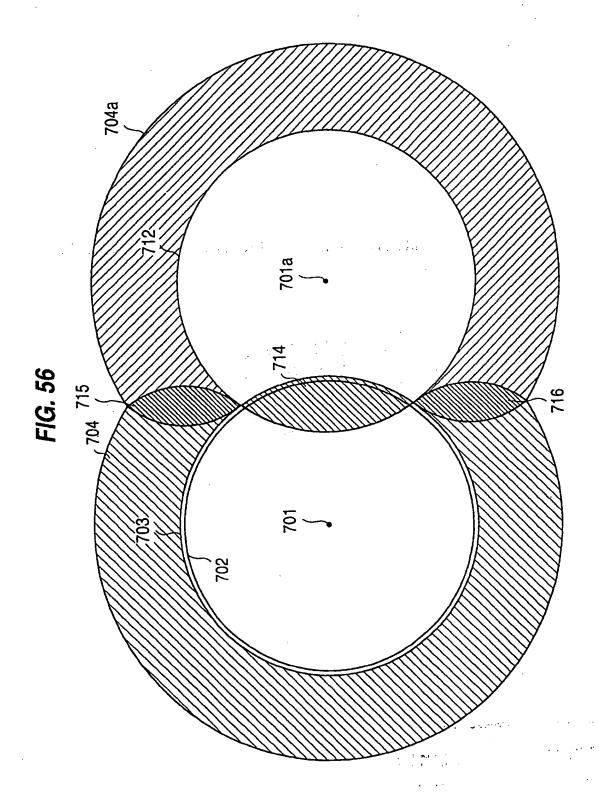


FIG. 57

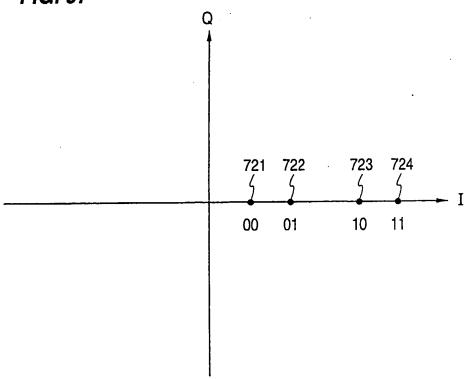
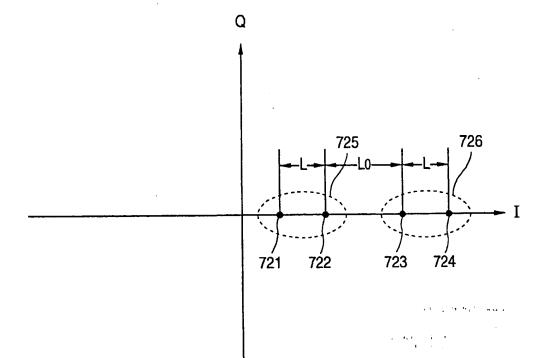
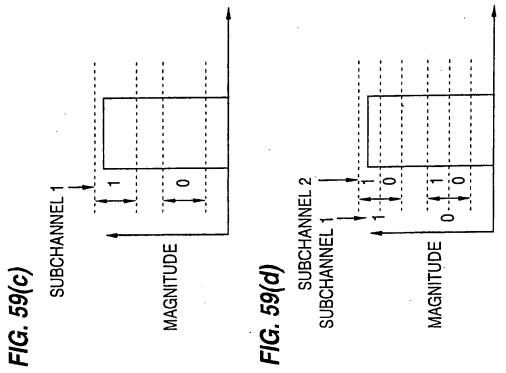
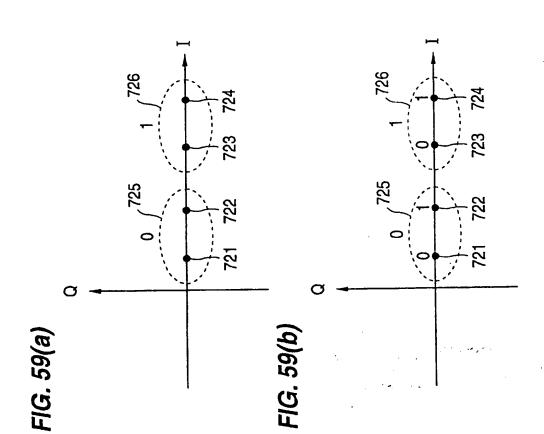


FIG. 58







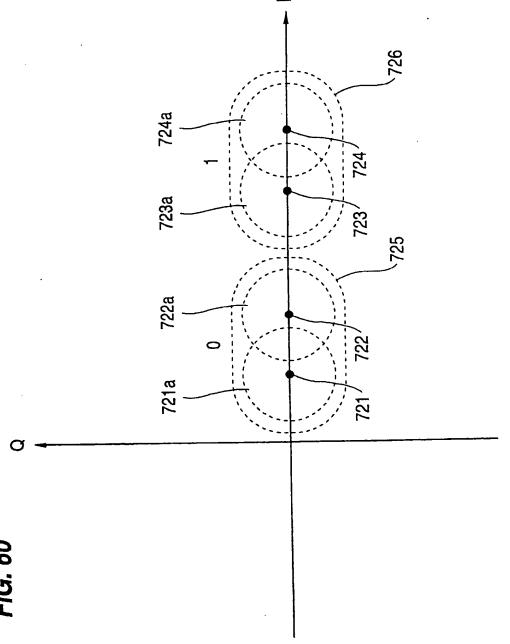
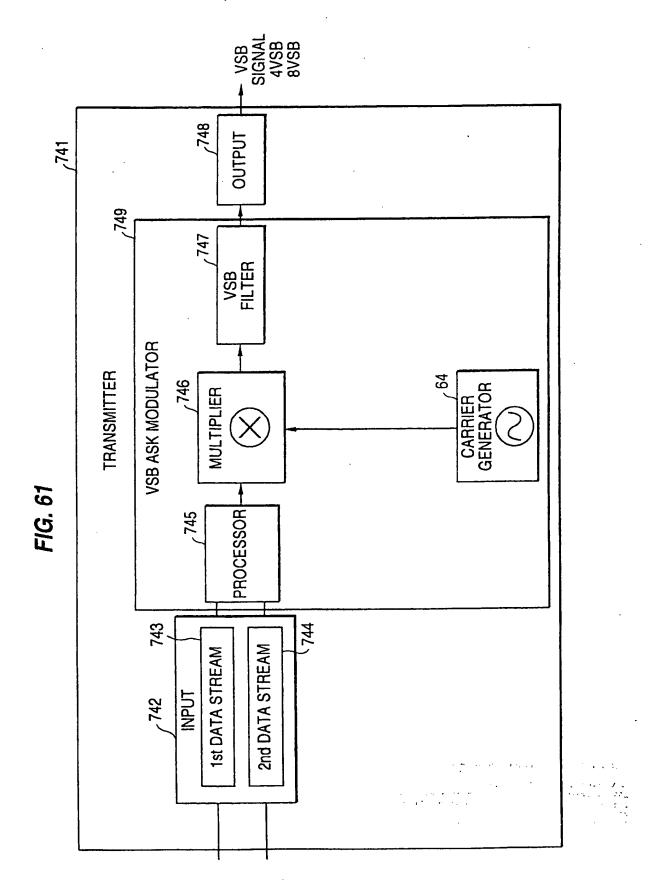
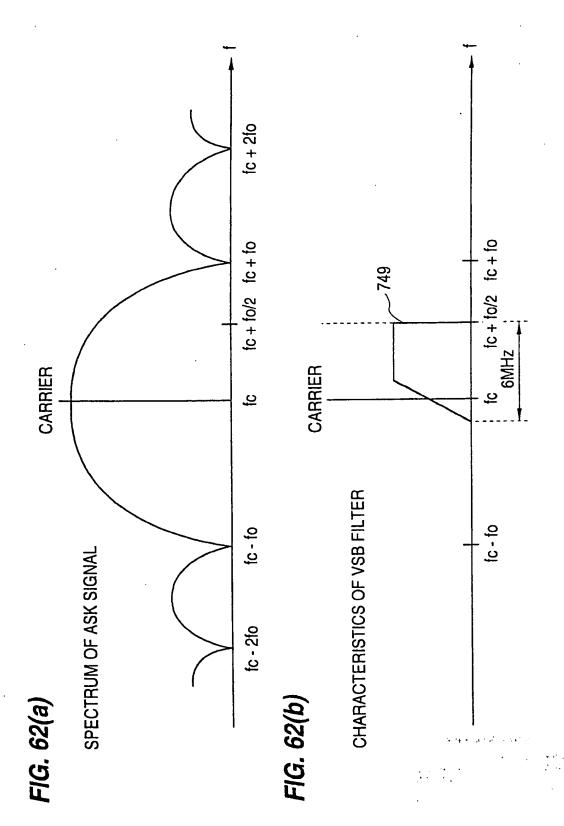
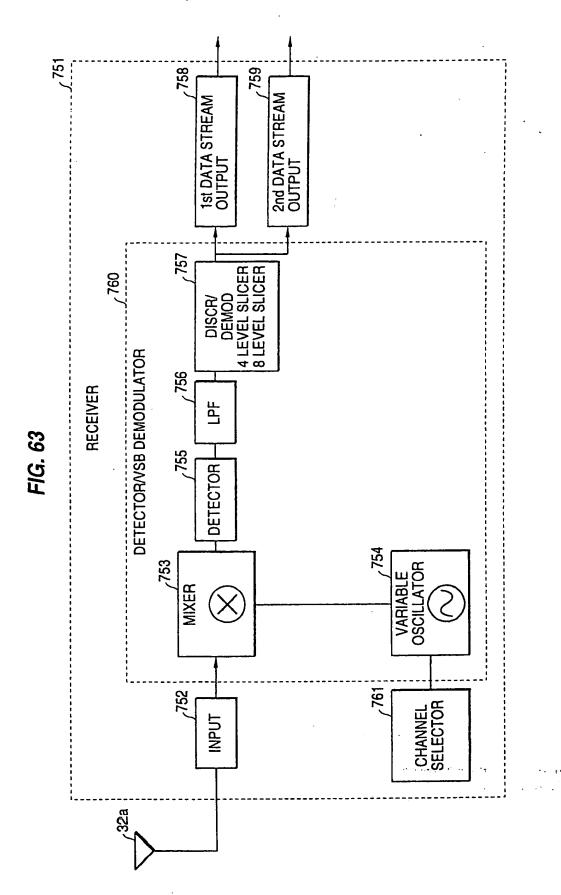
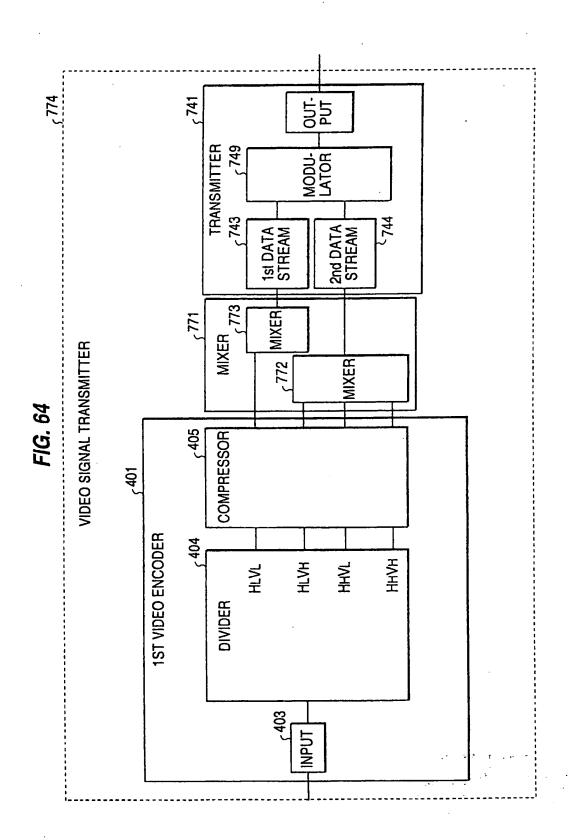


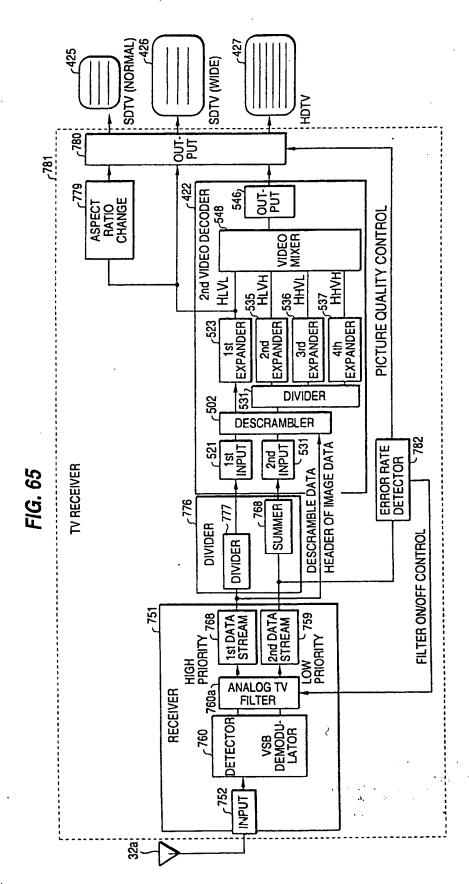
FIG. 60

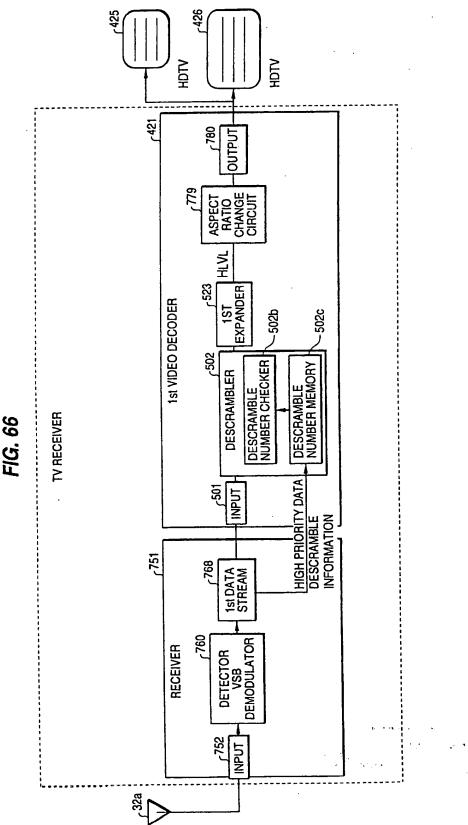


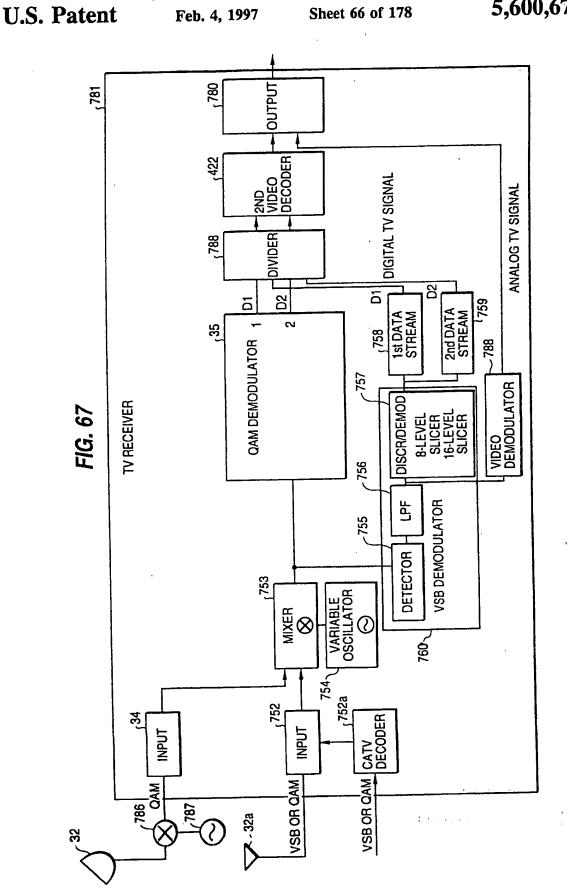


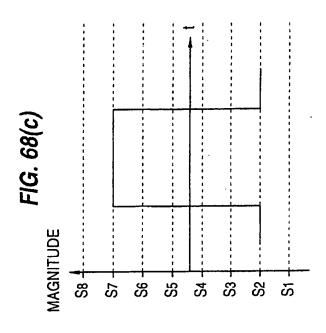


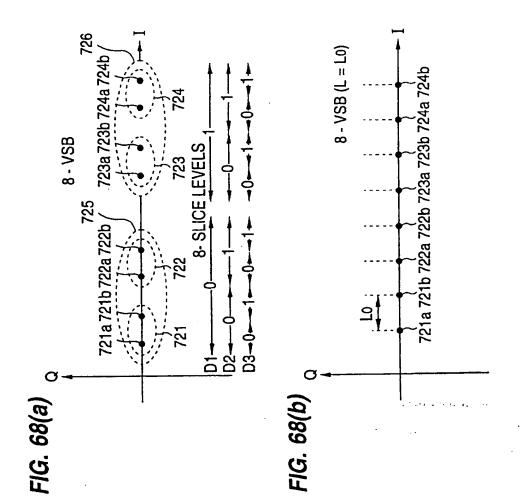


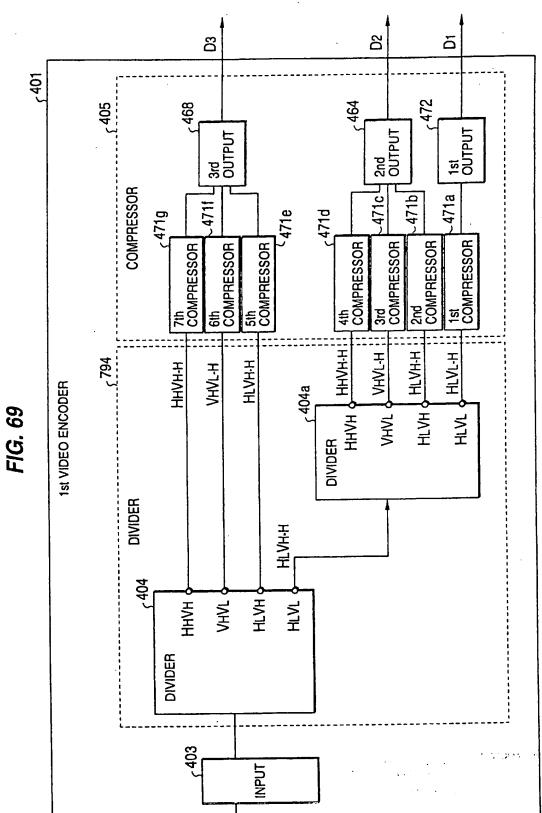


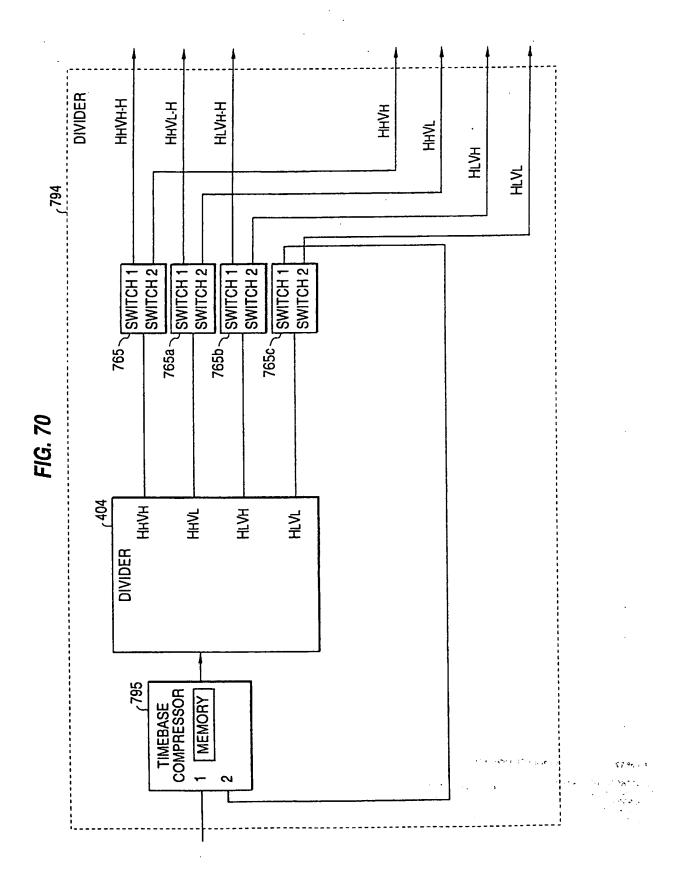




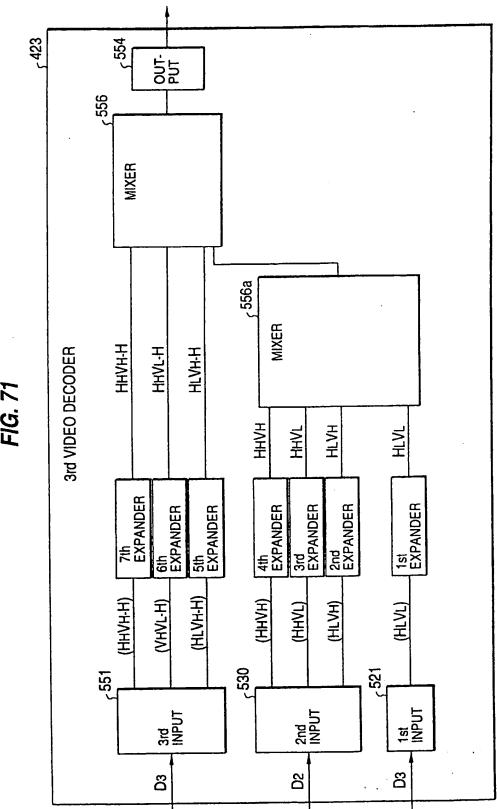








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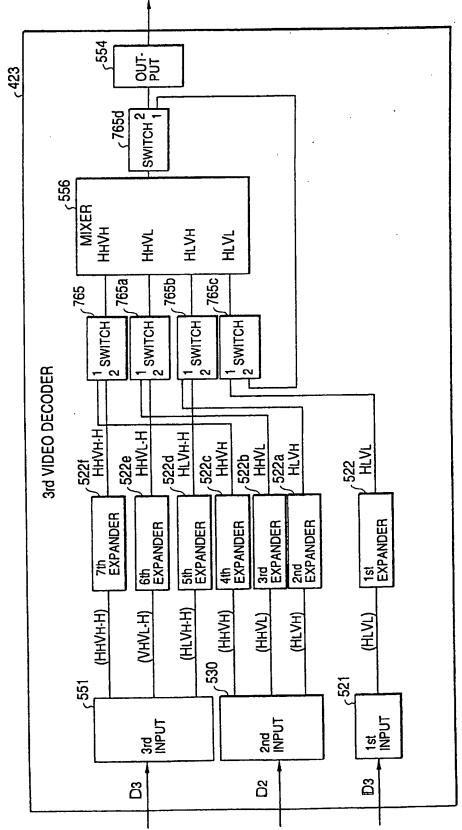


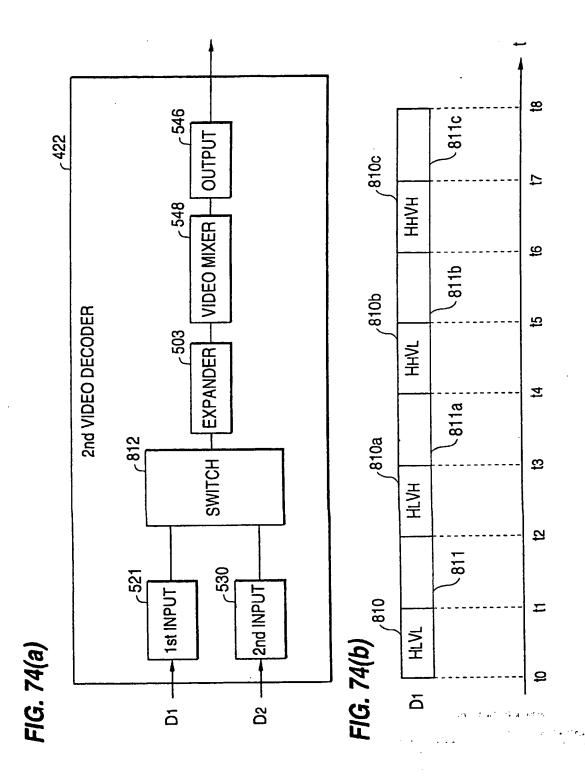
FIG. 72

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FIG. 73

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					112
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		HLVL			
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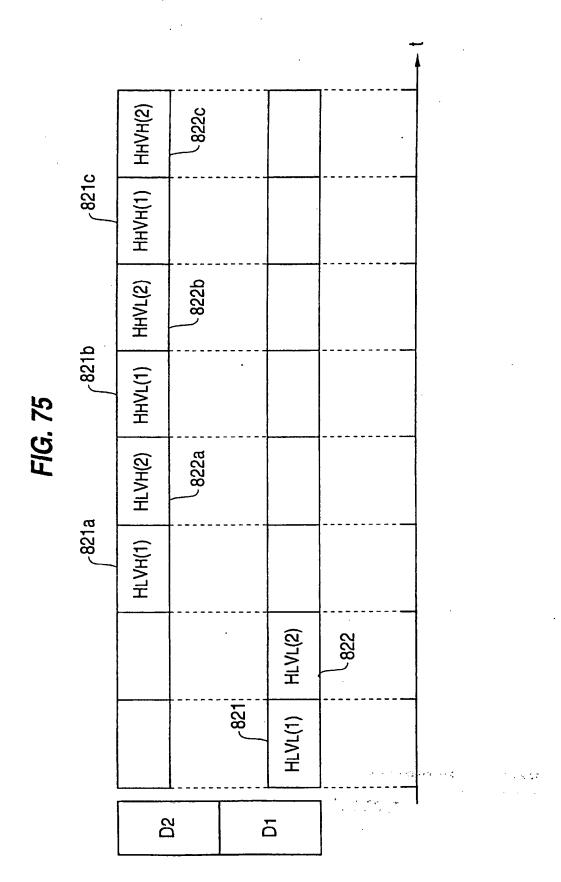
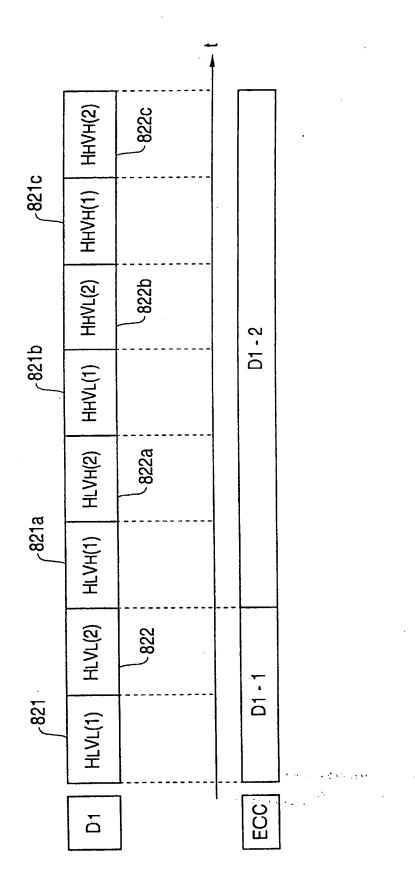


FIG. 76



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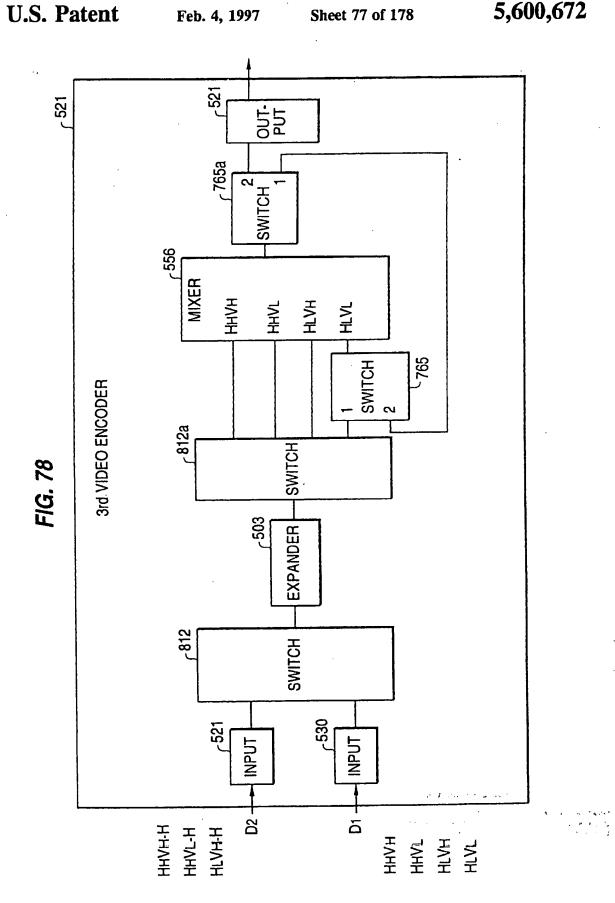
5

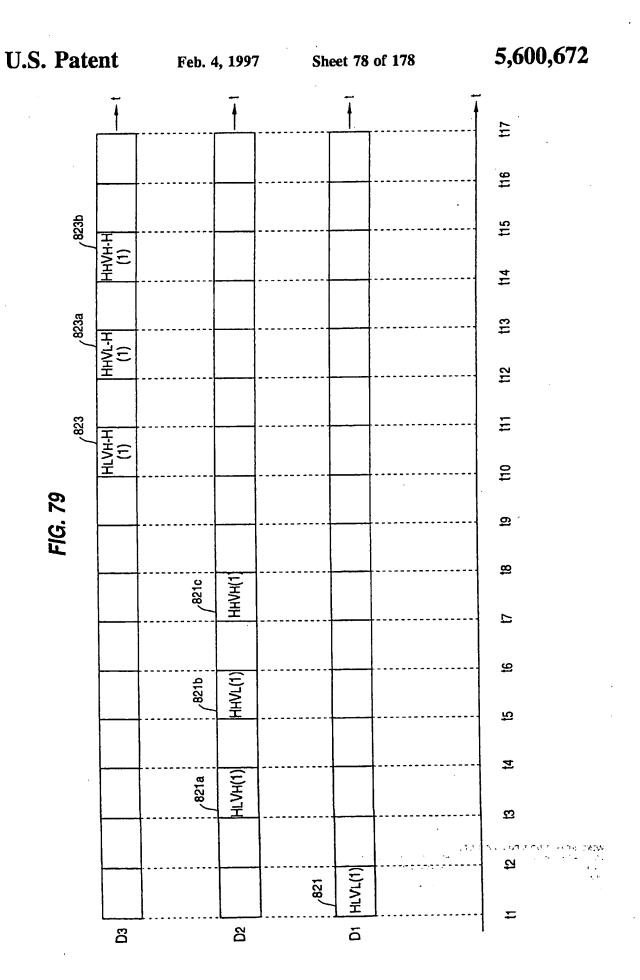
9

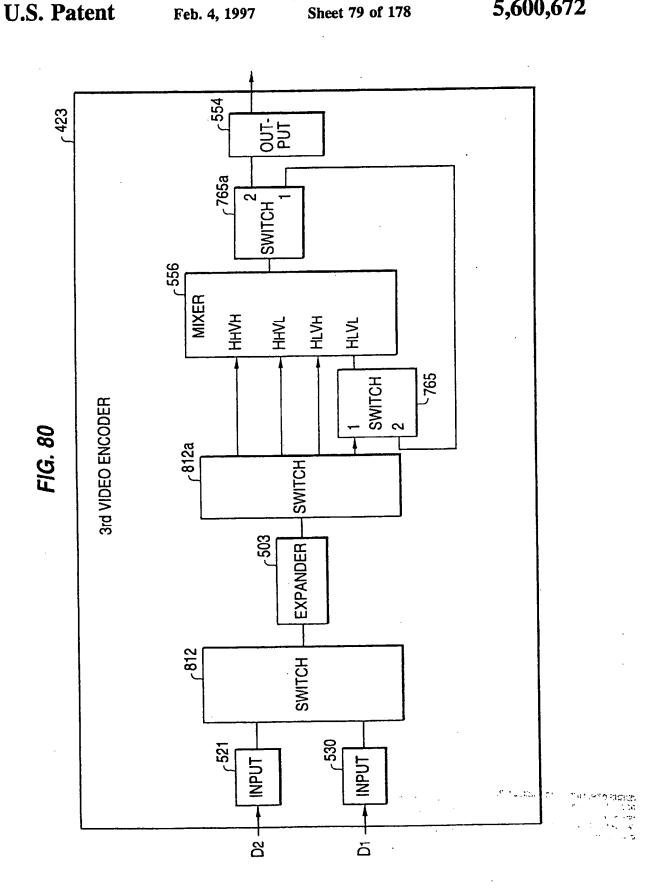
¥

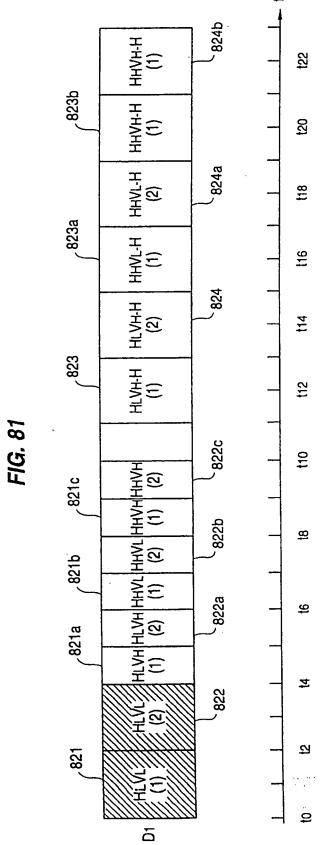
ស

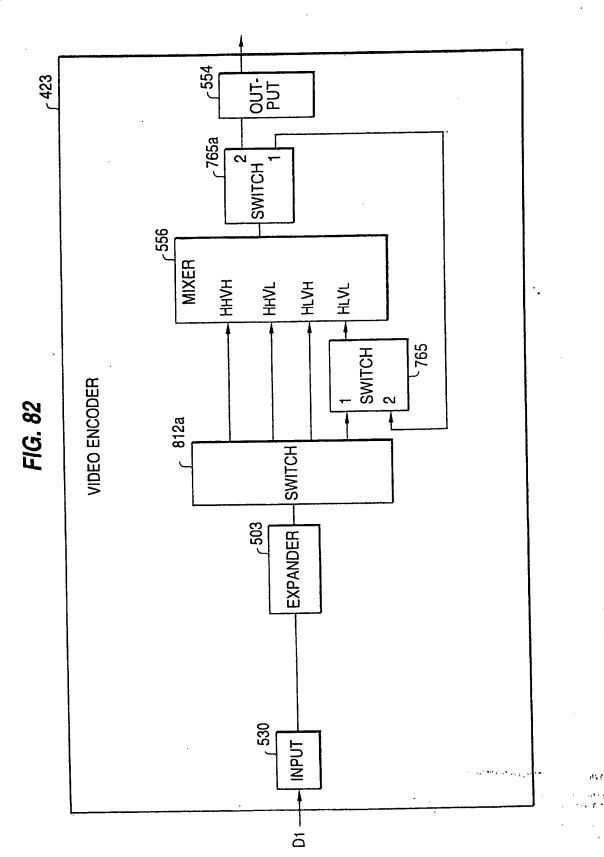
8

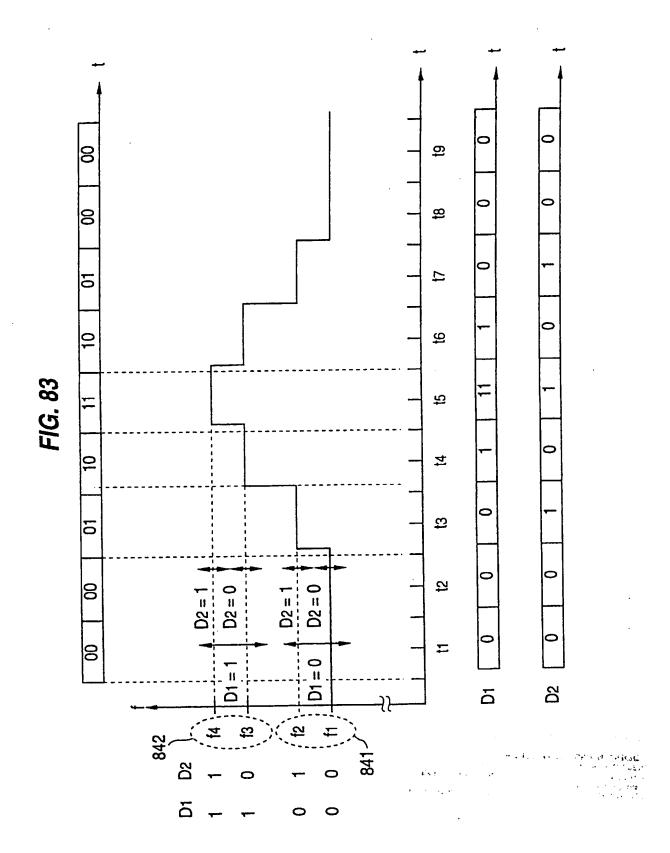


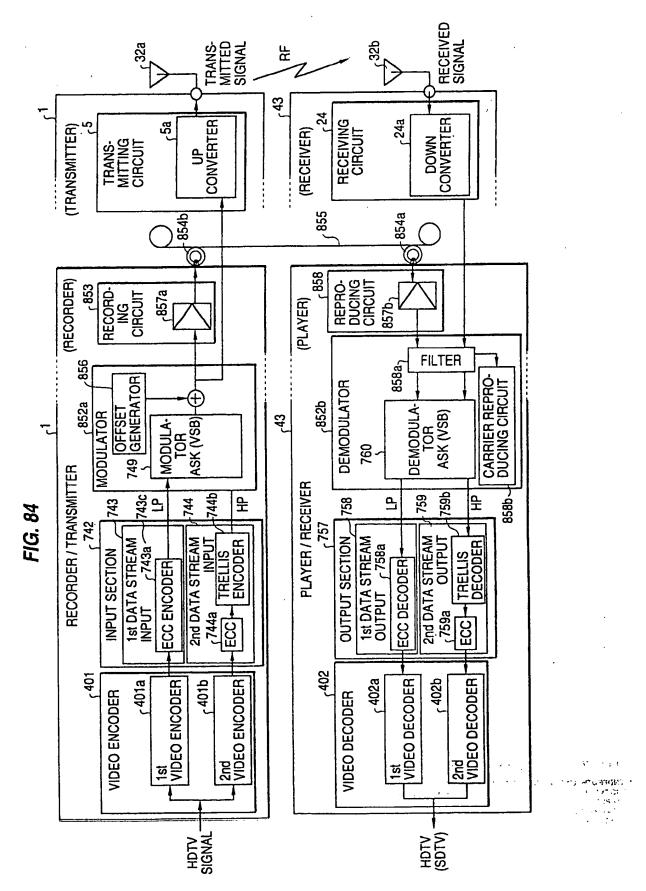


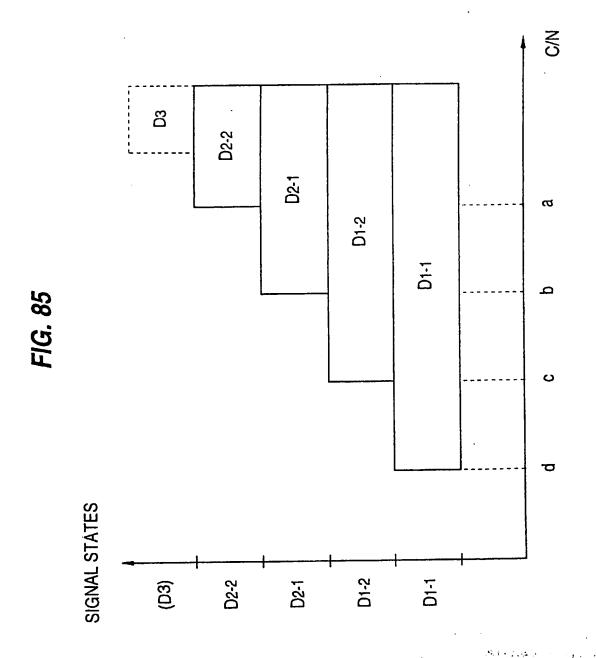


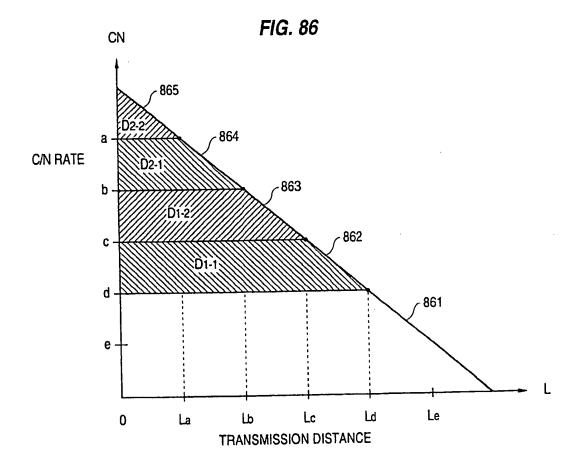


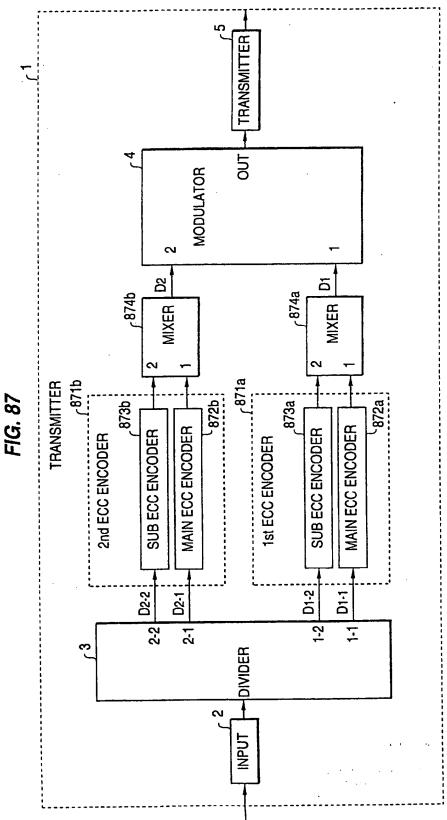












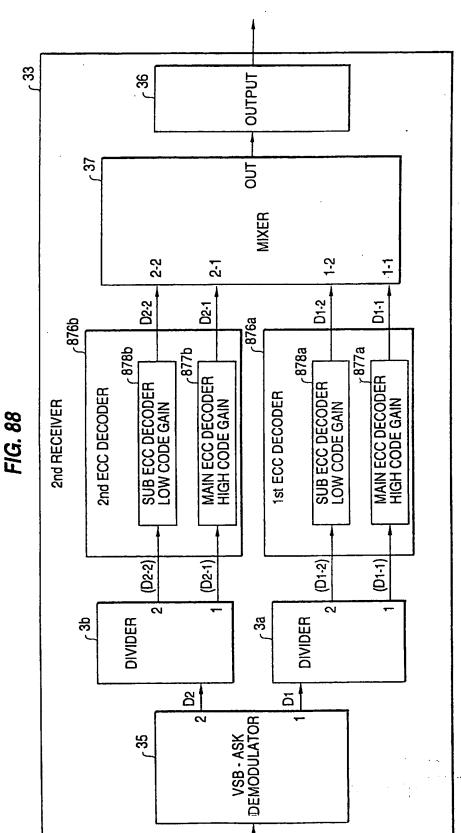
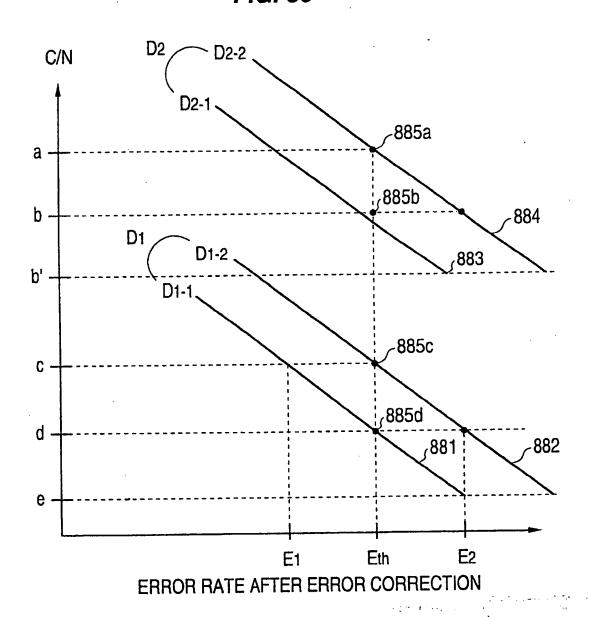


FIG. 89



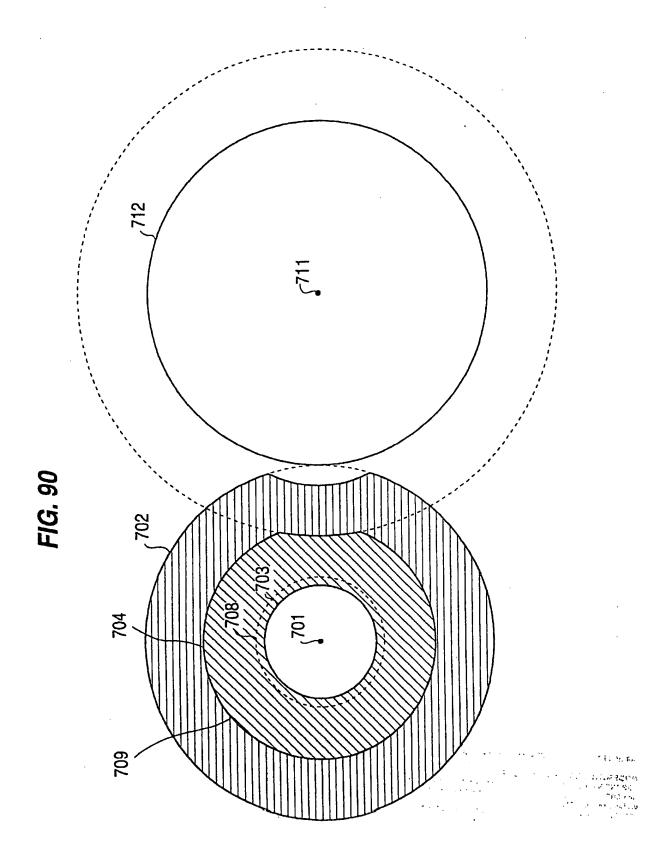
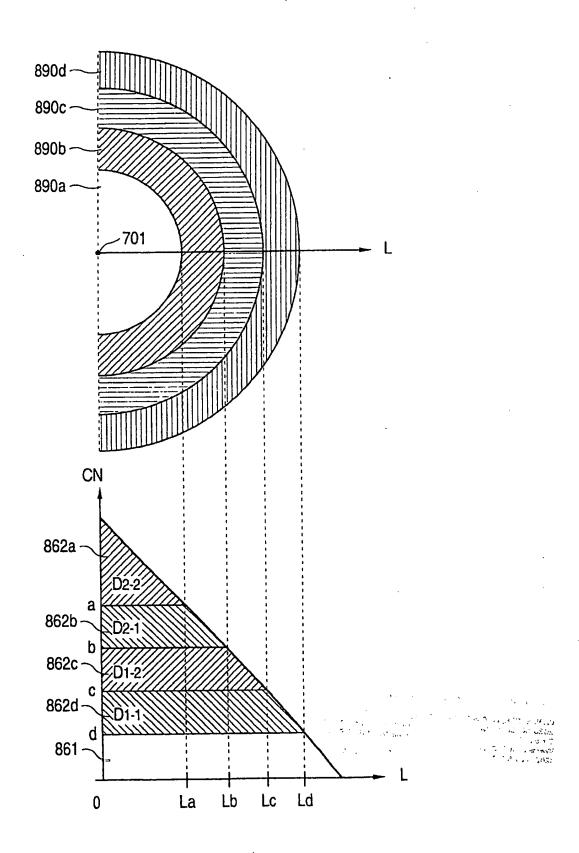
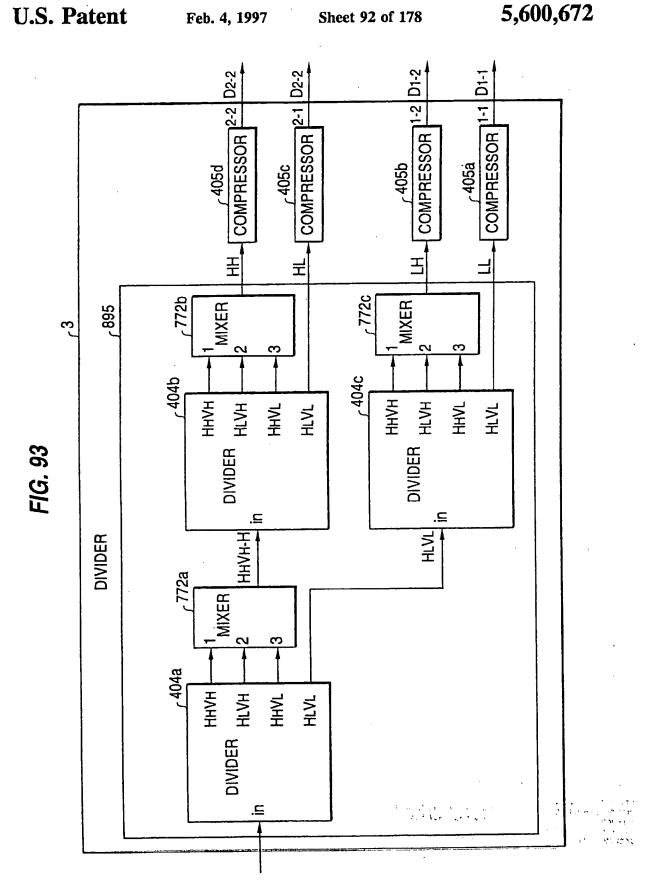


FIG. 92





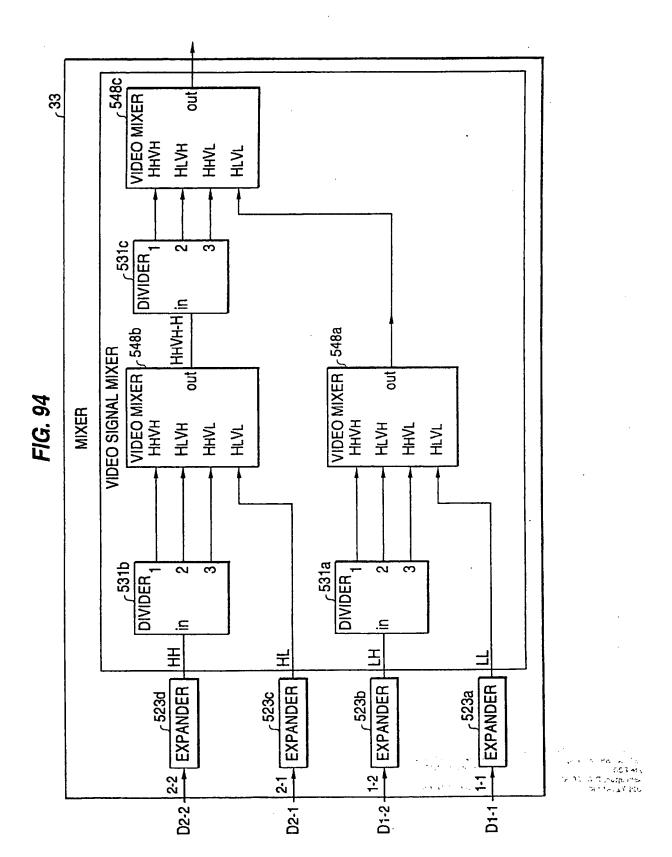
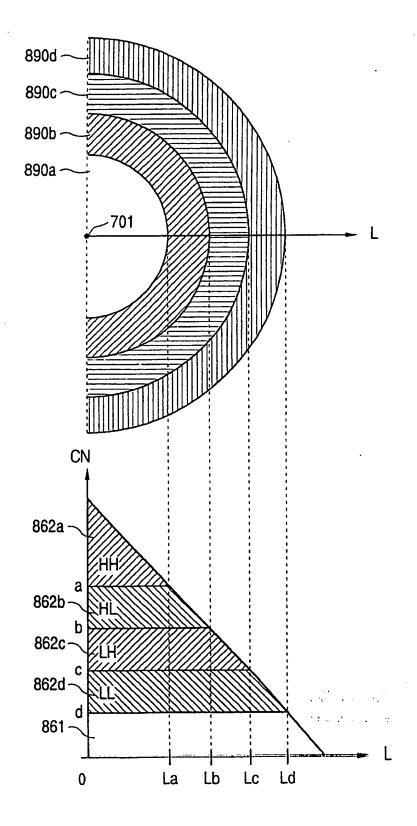
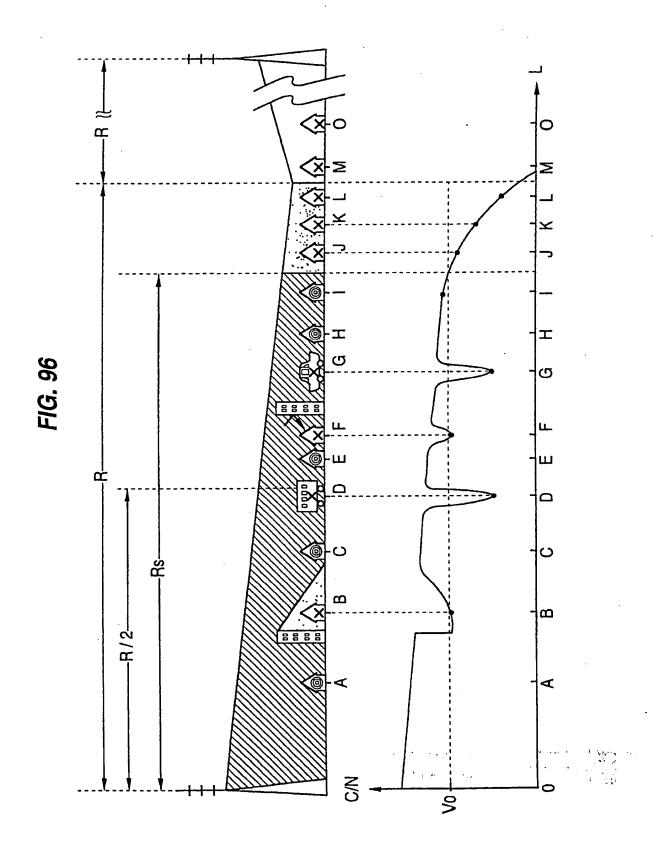


FIG. 95





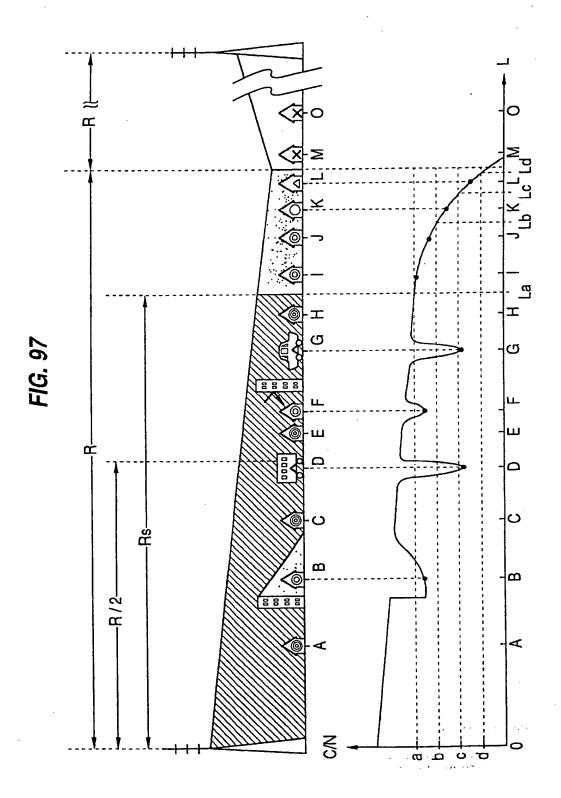


FIG. 98

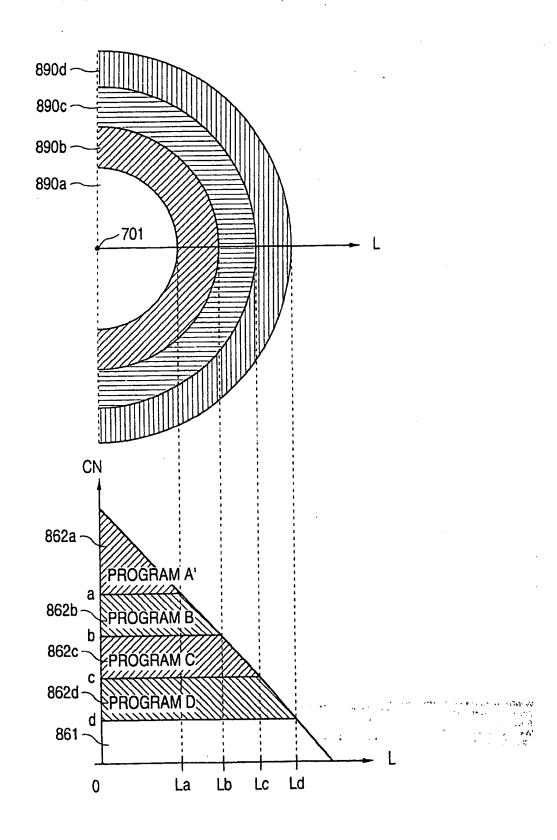


FIG. 99 ·85a 2δ 86 83b -86a 83a -2δ-0

FIG. 100

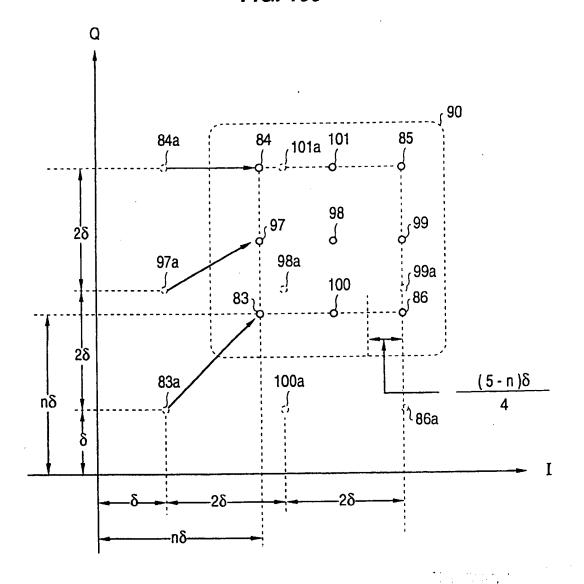


FIG. 101

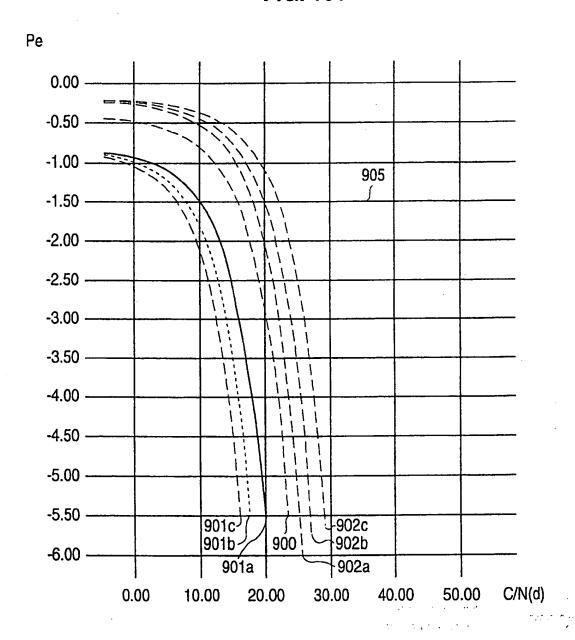


FIG. 102

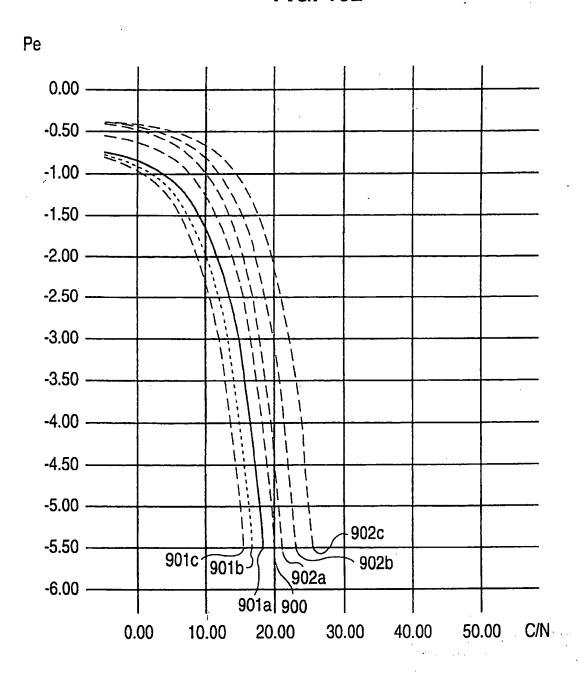


FIG. 103

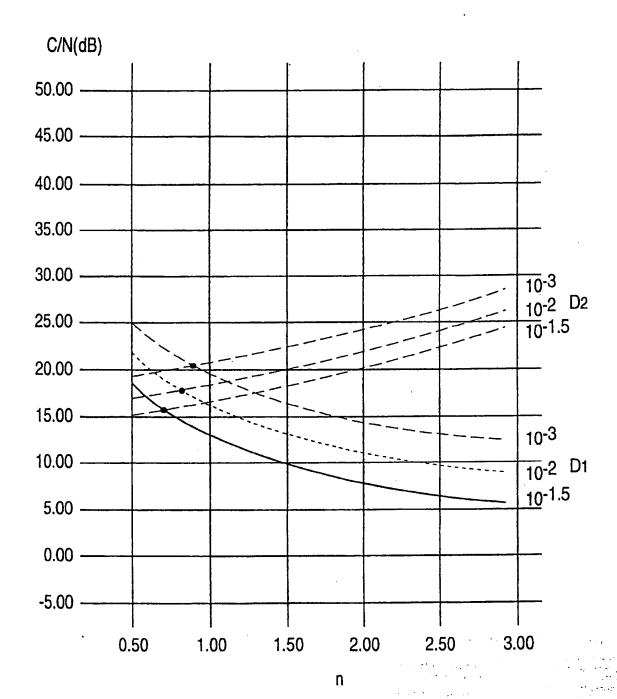
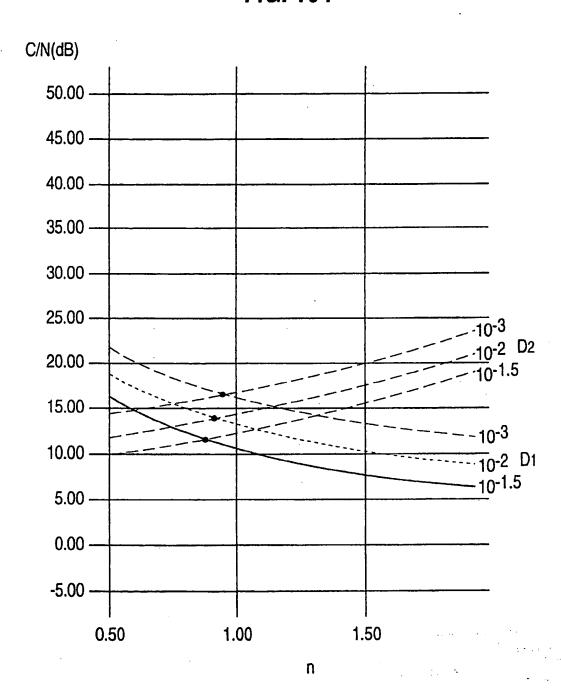
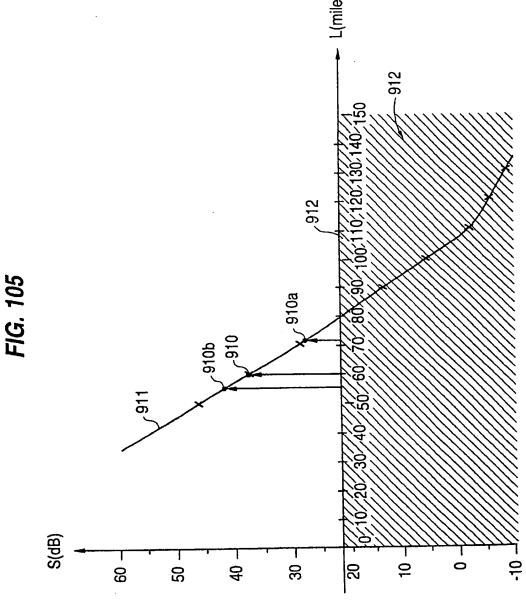
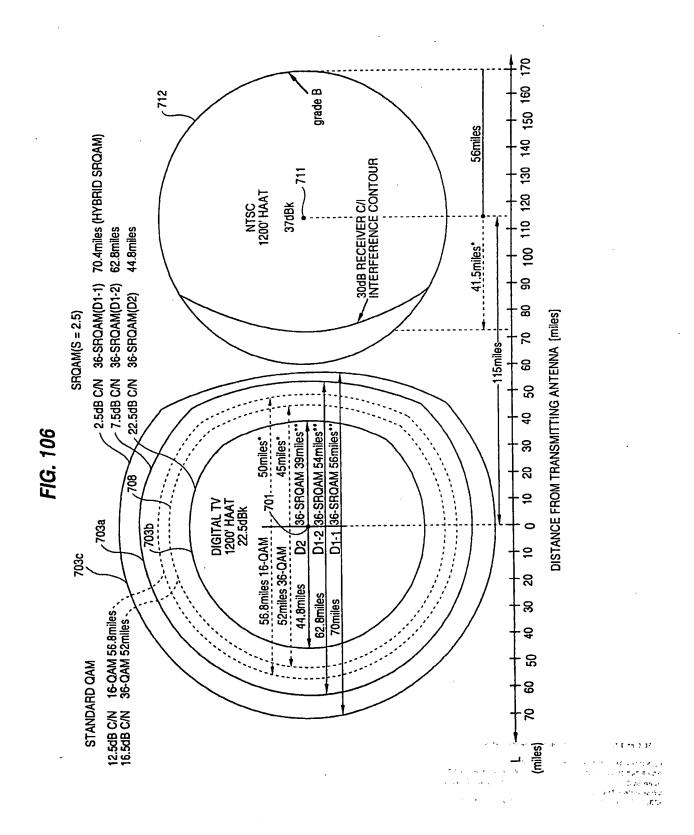


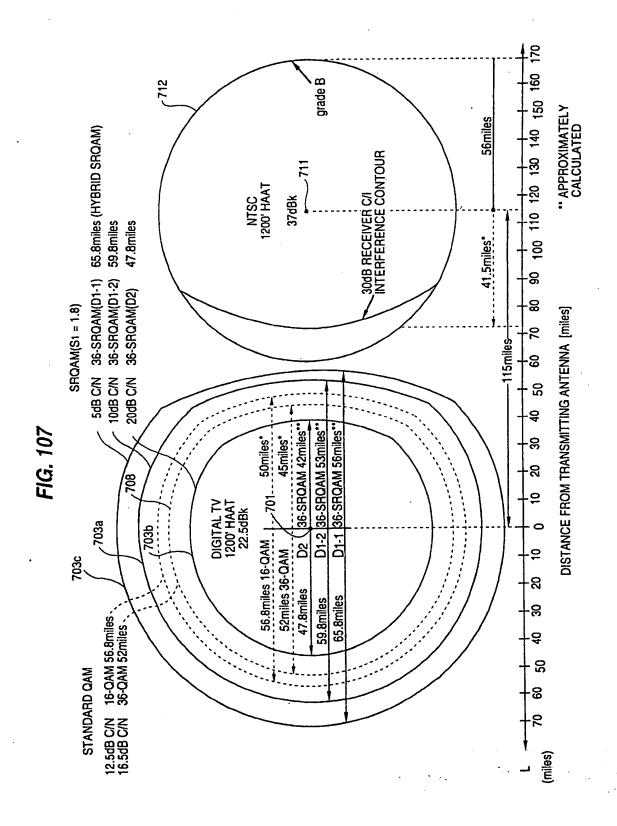
FIG. 104

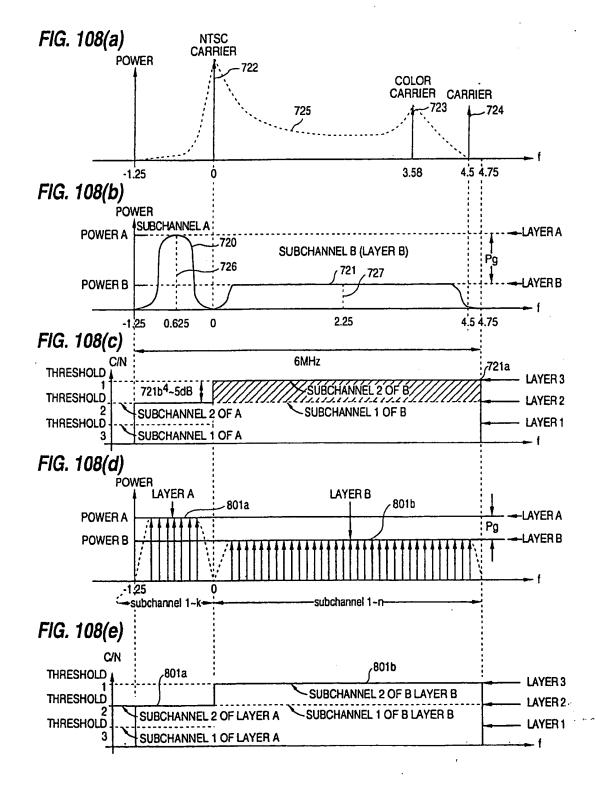


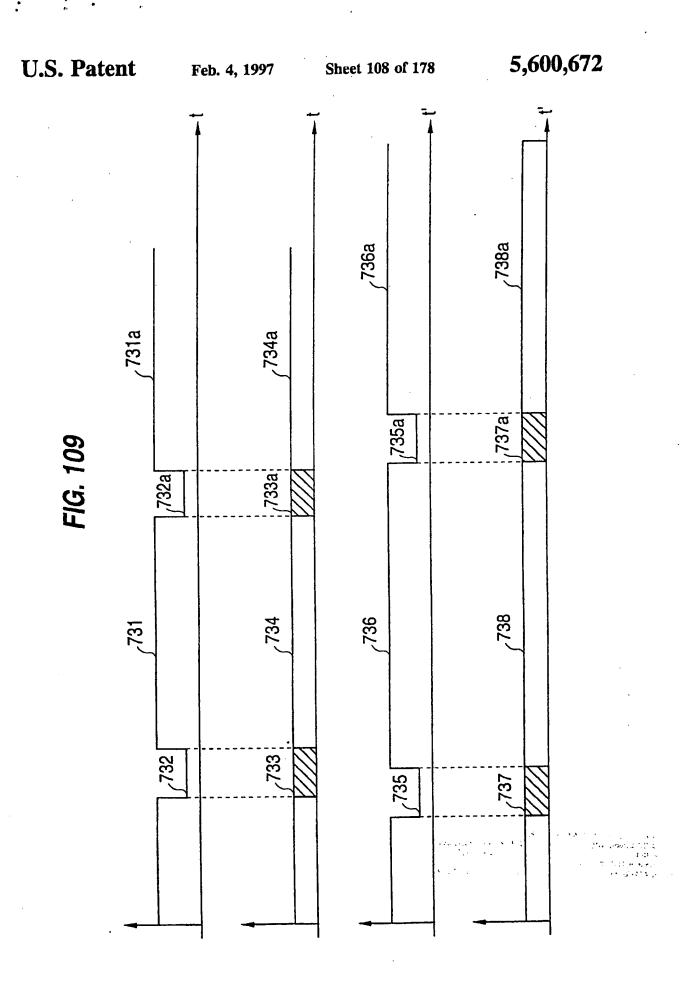




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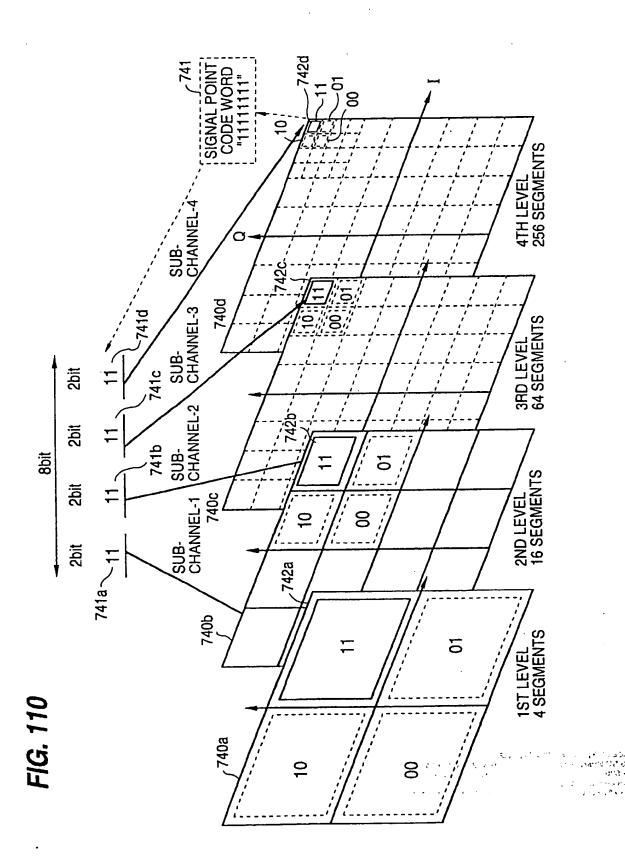


FIG. 111

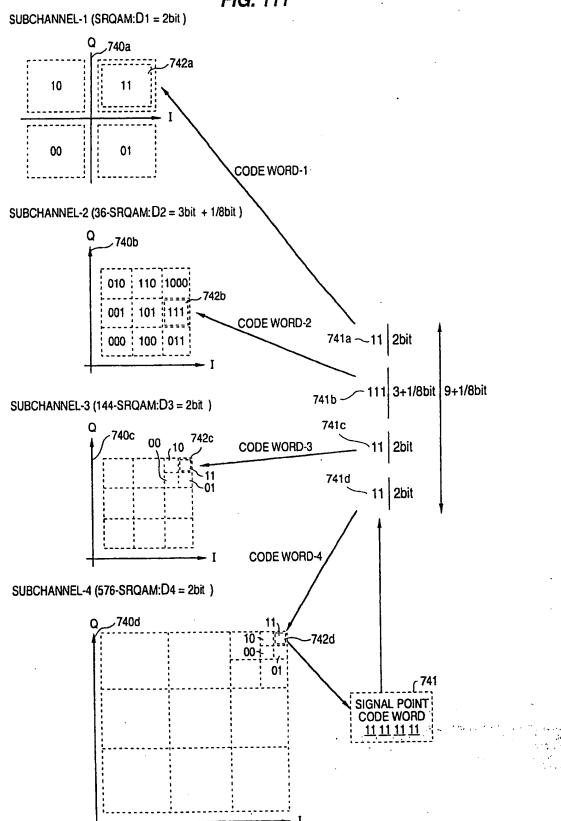
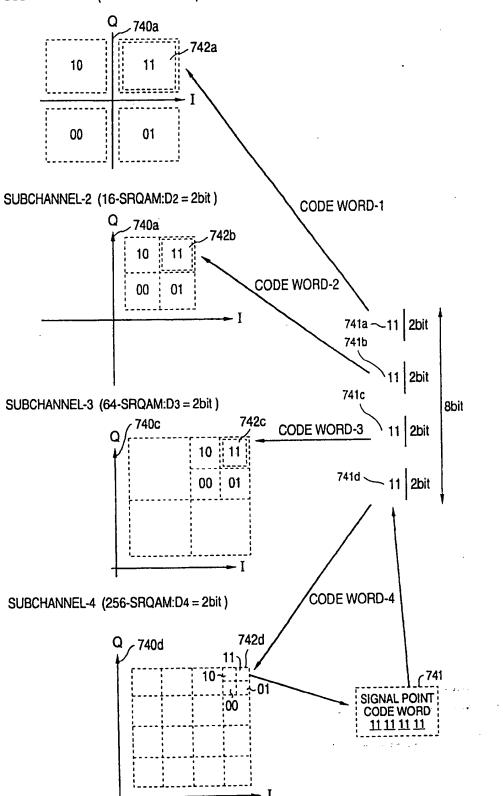
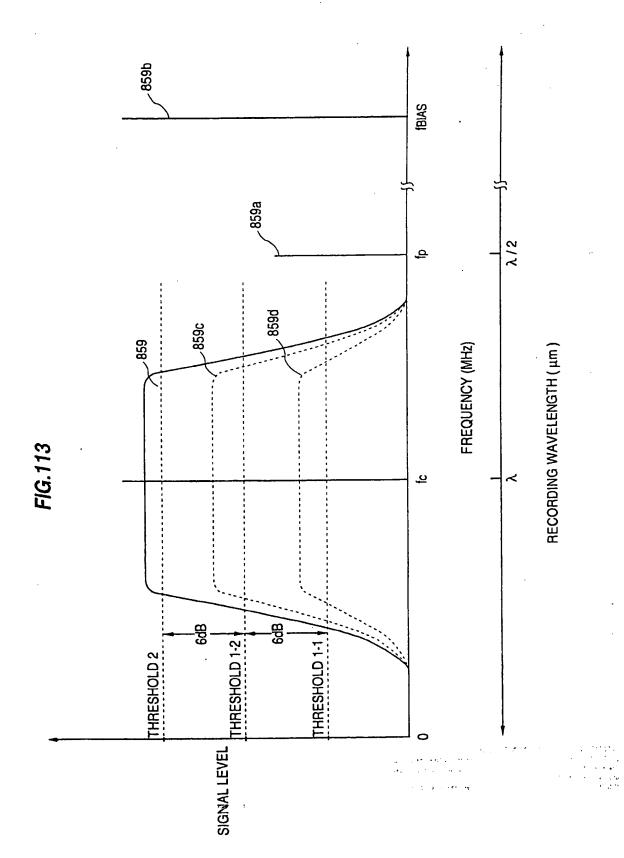
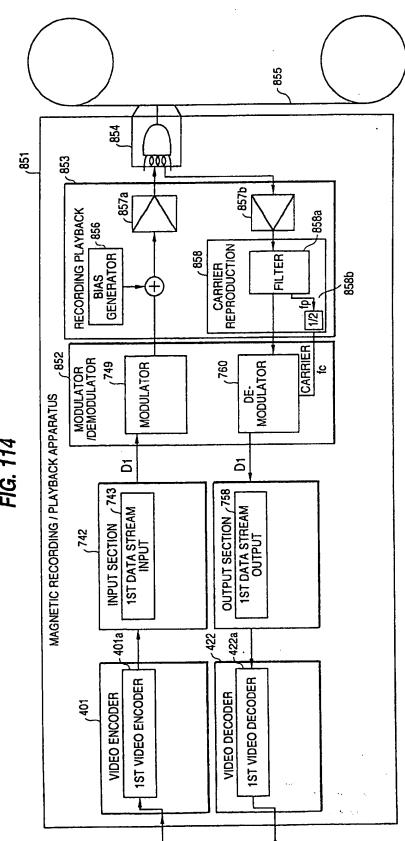


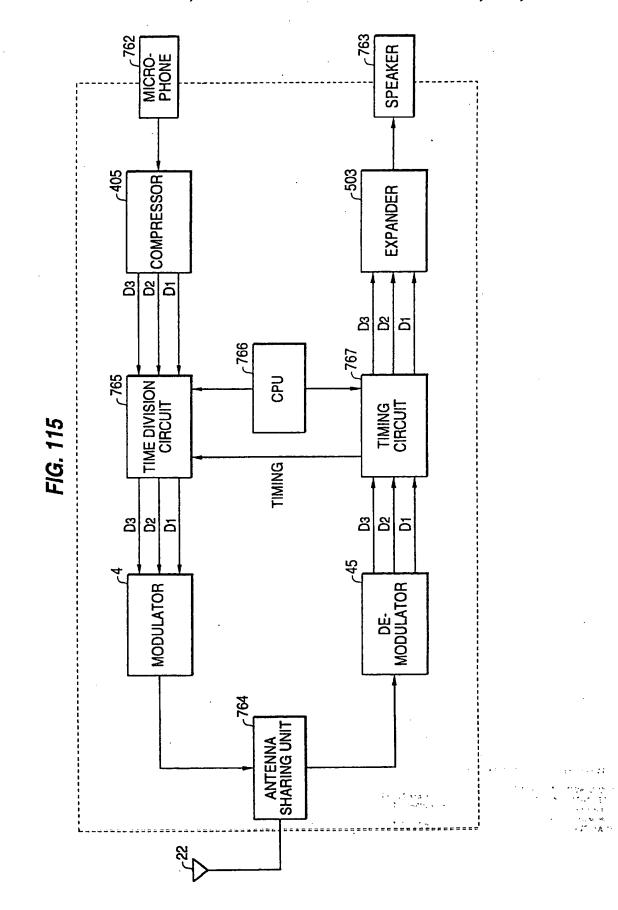
FIG. 112

SUBCHANNEL-1 (SRQAM:D1 = 2bit)



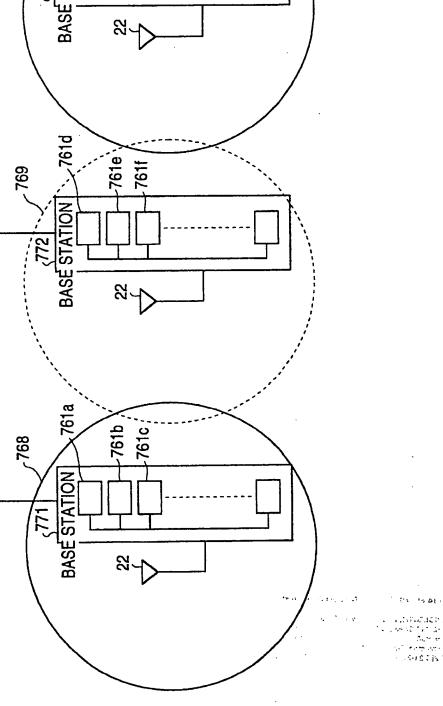


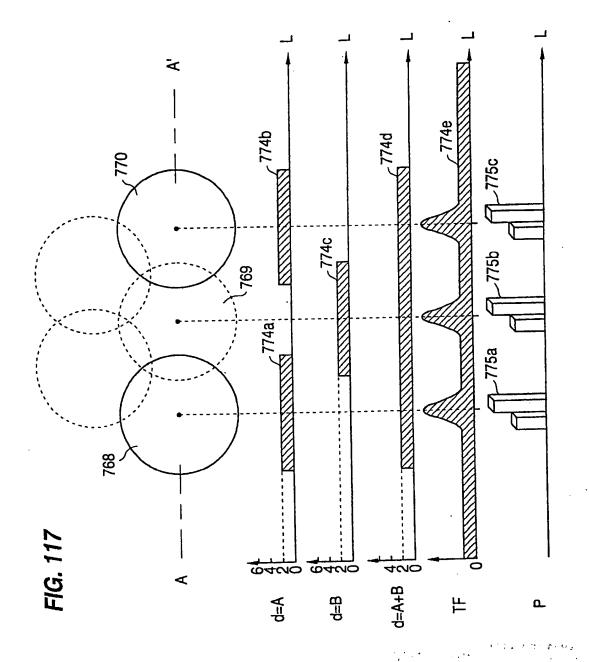


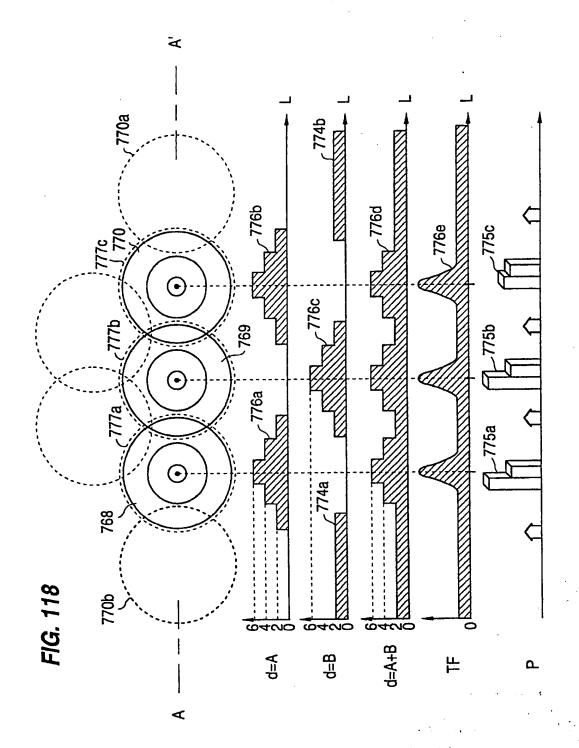


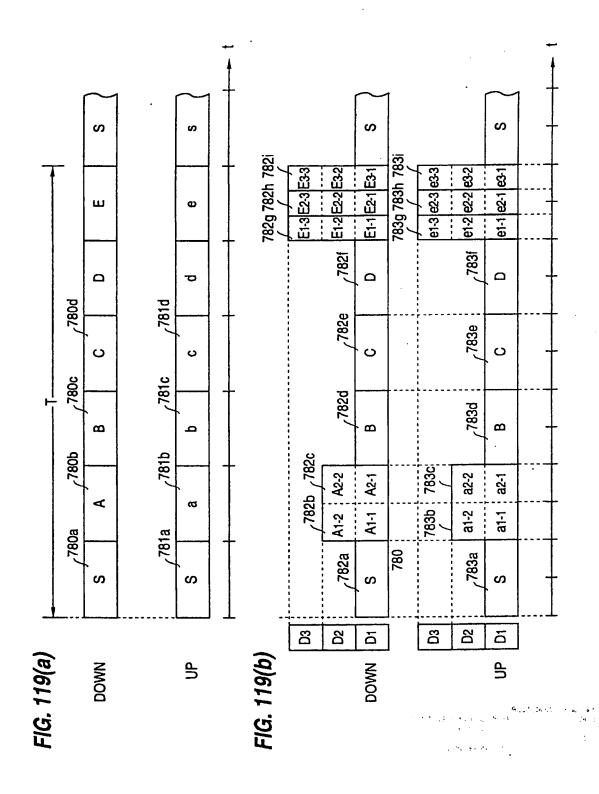


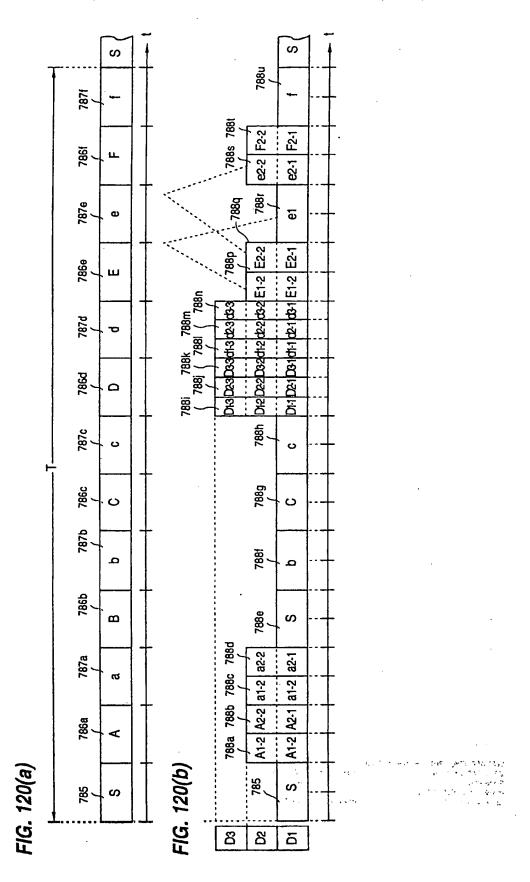
BASE STATION CONTROLLER

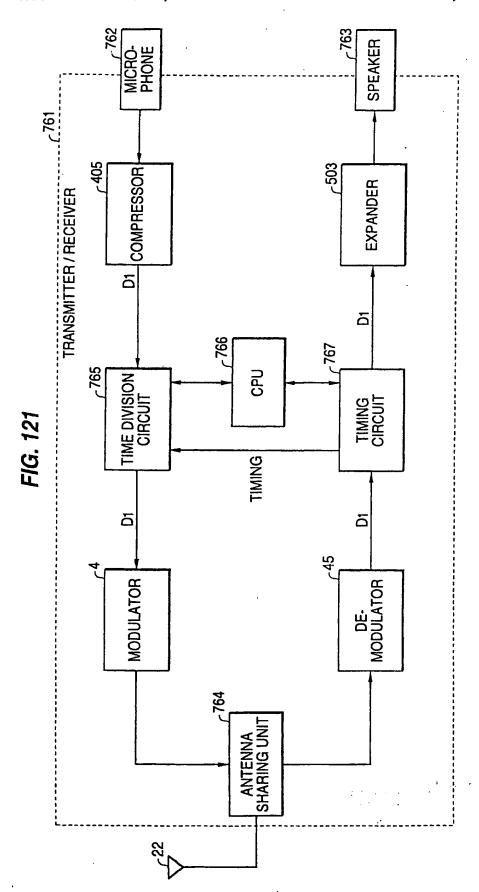


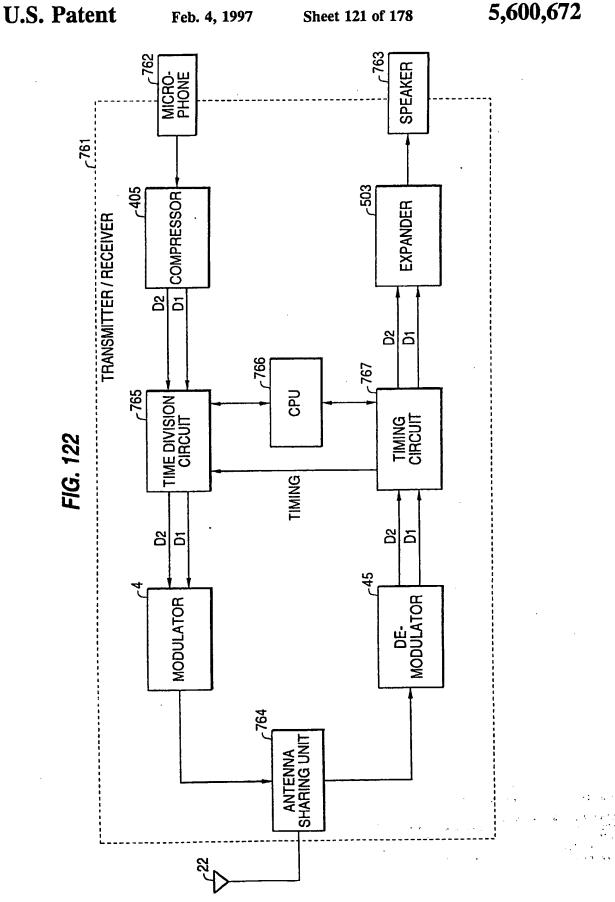


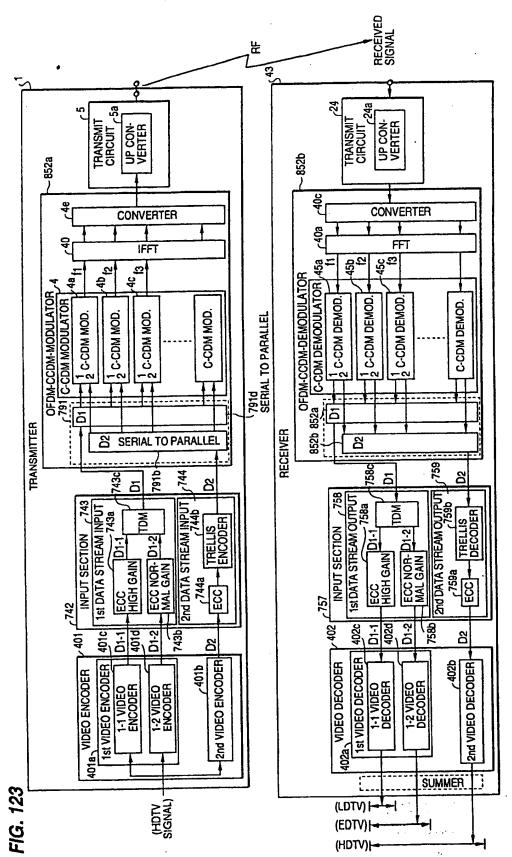


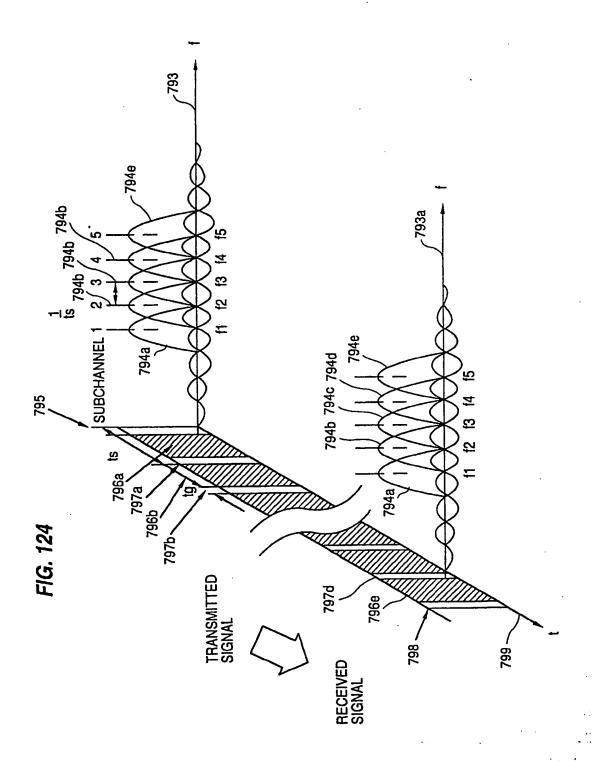


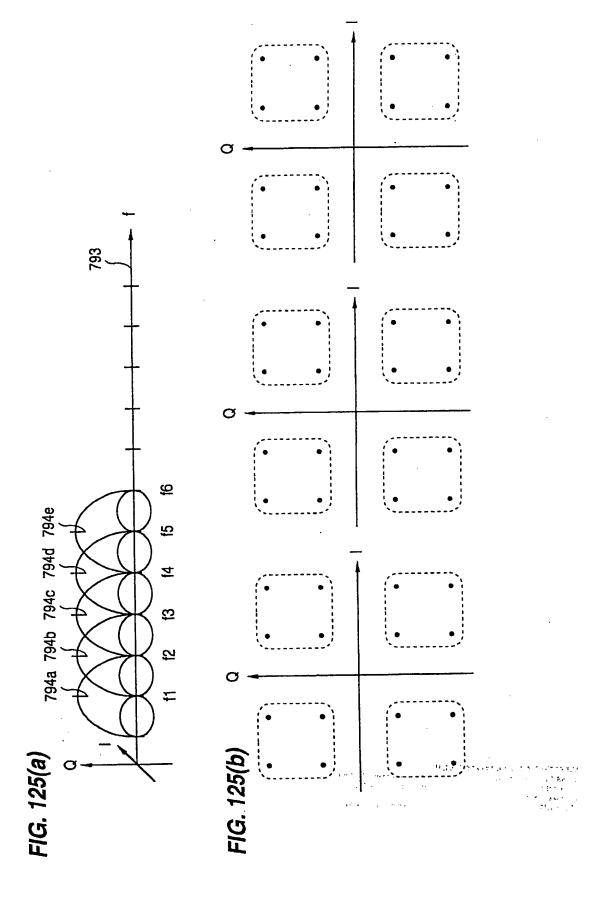


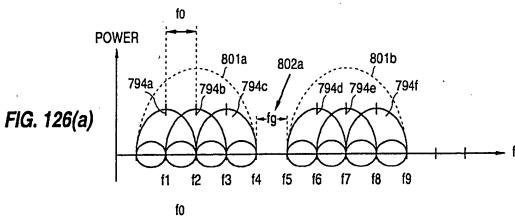


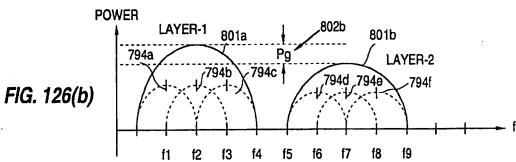


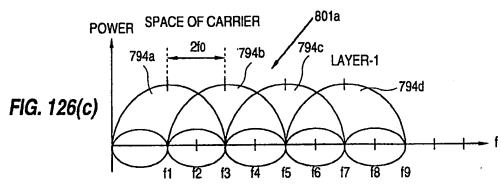


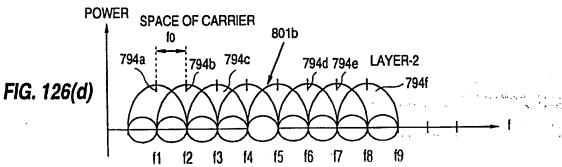












-24a ↑ RECEIVED SIGNAL 胎 43 DOWN CONVERTER UP CONVERTER 24 INPUT CIRCUIT DIVIDER **SUMMER 45** 45c **45a** 6 \$ C-CDM MODULATOR C-CDM DEMOD. MODULATOR DEMODULATOR C-CDM DEMODULATOR C-CDM DEMOD. C-CDM DEMOD. C-CDM DEMOD. с-срм мор. C-CDM MOD. C-CDM MOD. C-CDM MOD 791 TRANSMITTER RECEIVER PARALLEL TO SERIAL CONVERTER SERIAL TO PARALLEL CONVERTER 758c .743c 742 , 757 .758 759 743 ដ 2nd DATA STREAM INPUT 1st DATA STREAM OUTPUT 2nd DATA STREAM OUTPU 1st DATA STREAM INPUT TRELLIS **OUTPUT SECTION** ECC NOR- D1-2 MAL GAIN ECC NOR- D1-2 MAL GAIN INPUT SECTION ECC HIGH GAIN HIGH GAIN ည္သ ECC 402d 401a 401c 402a 758b 401d 743b 8 6 402b 2nd VIDEO ENCODER 1st VIDEO ENCODER 1st VIDEO DECODER 2nd VIDEO DECODER VIDEO ENCODER VIDEO DECODER 1-1 VIDEO ENCODER 1-2 VIDEO ENCODER 1-1 VIDEO DECODER 1-2 VIDEO DECODER (LDTV) |-(EDTV) (HDTV)

FIG. 127

FIG. 128(a)

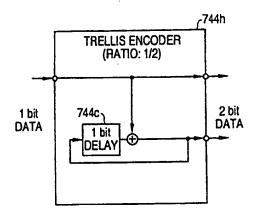


FIG. 128(d)

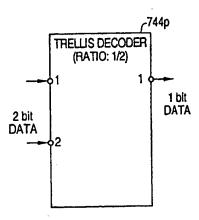


FIG. 128(b)

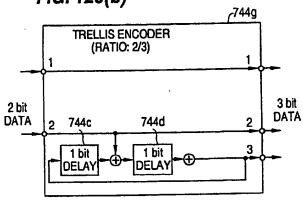


FIG. 128(e)

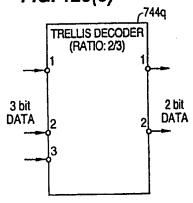


FIG. 128(c)

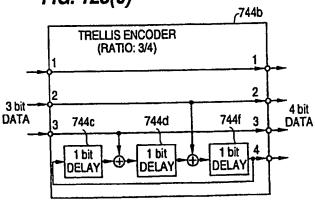
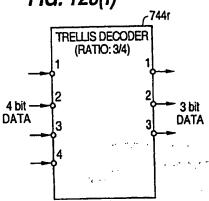
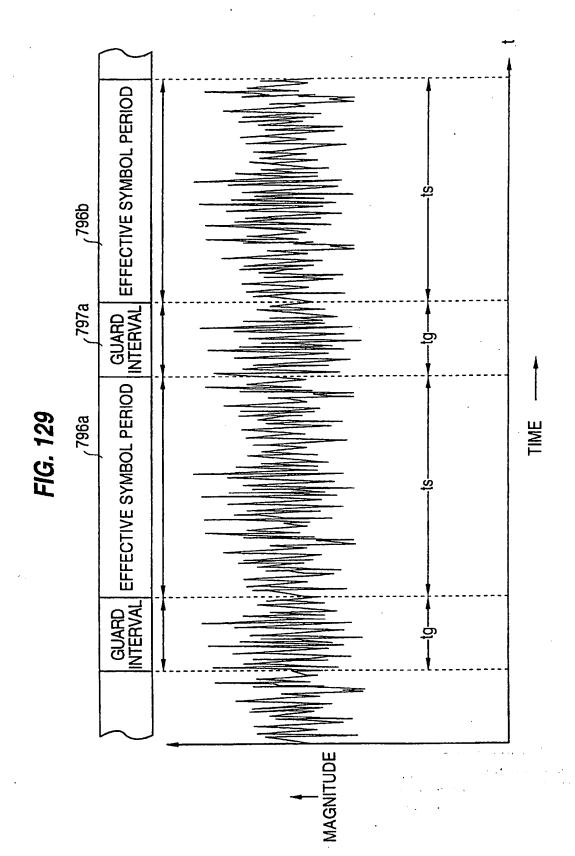


FIG. 128(f)







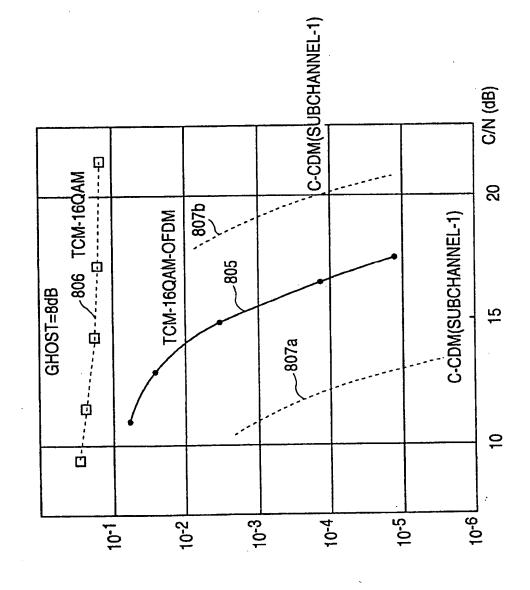


FIG. 130

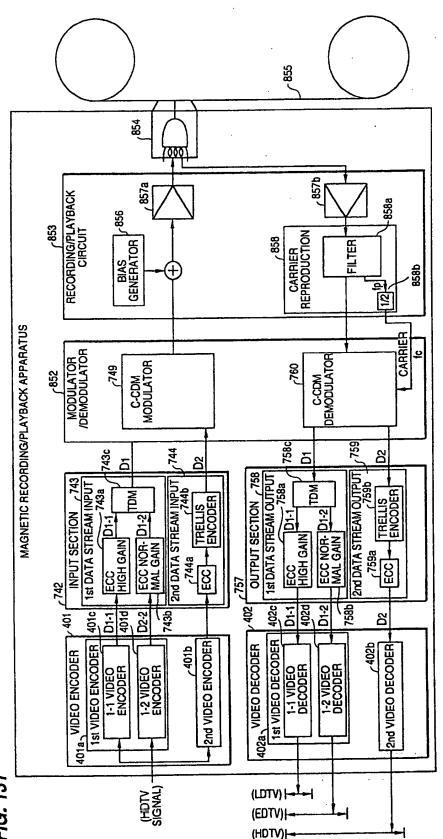
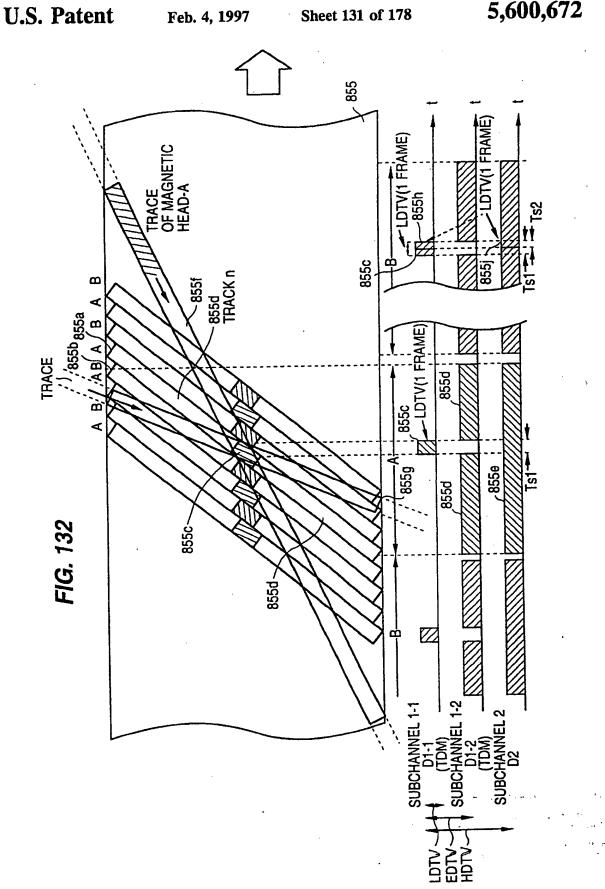
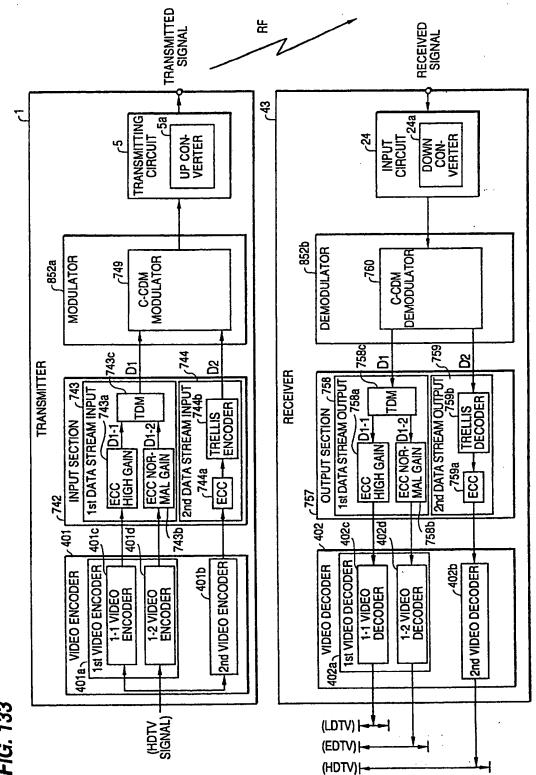
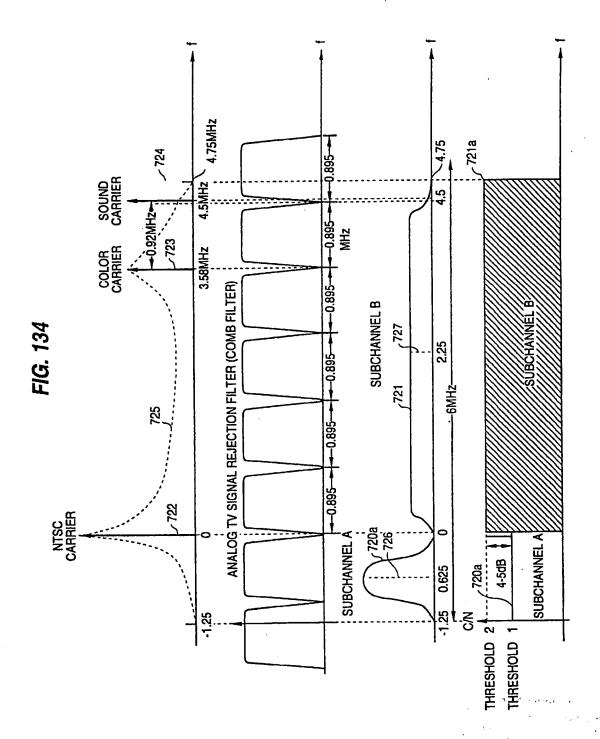


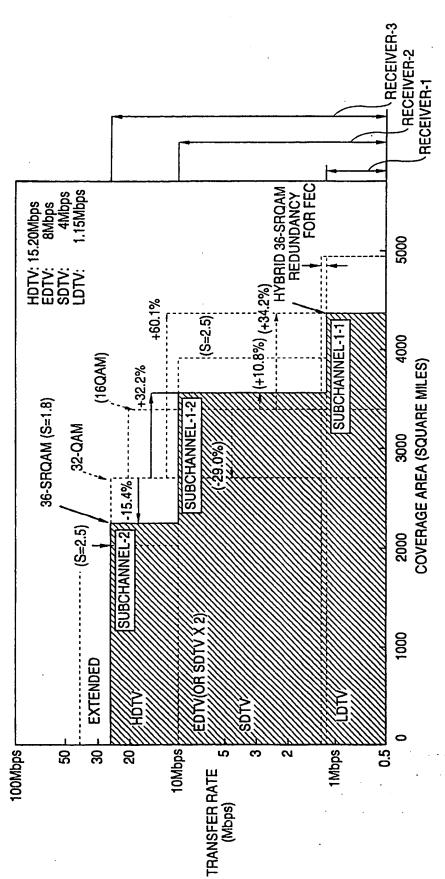
FIG. 131

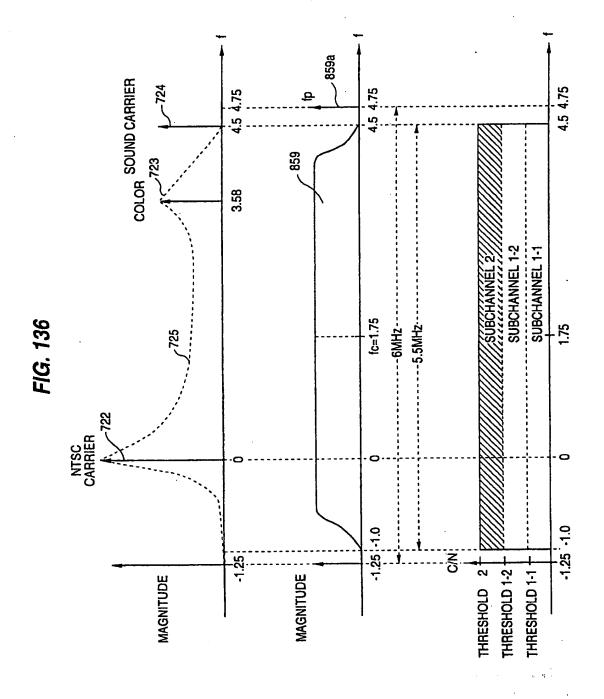












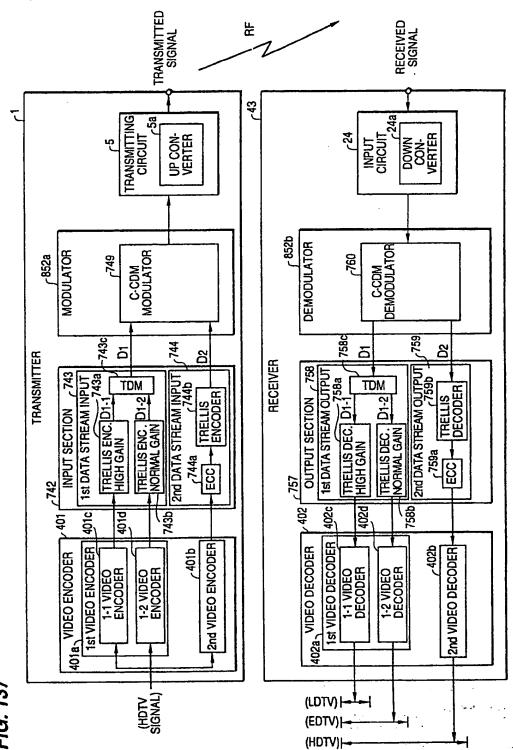


FIG. 137

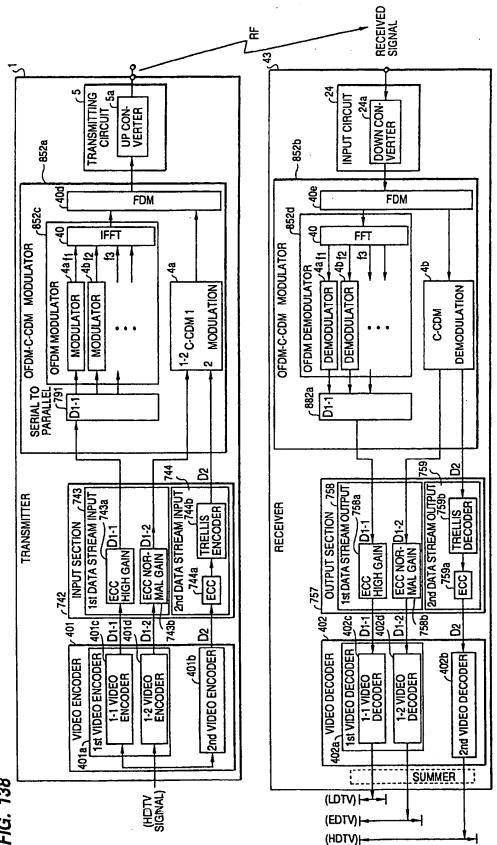


FIG. 139

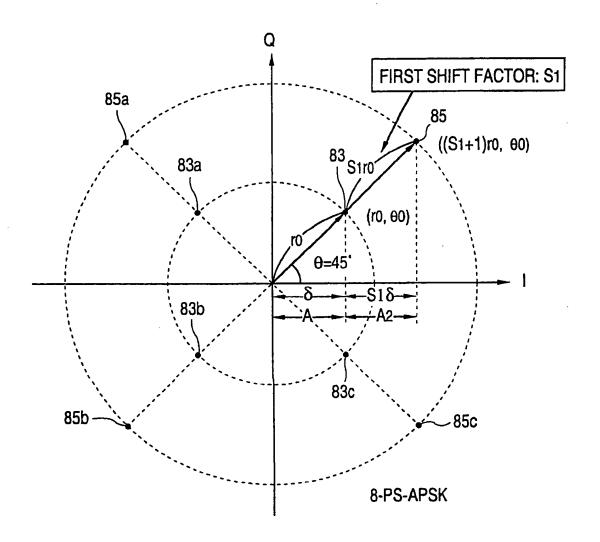


FIG. 140

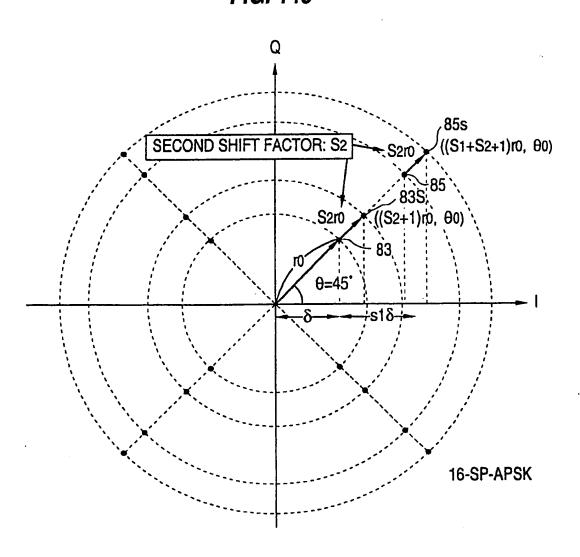


FIG. 141

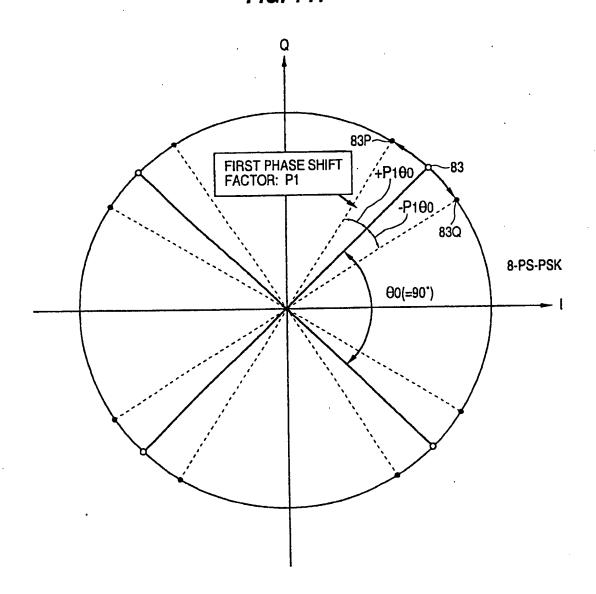
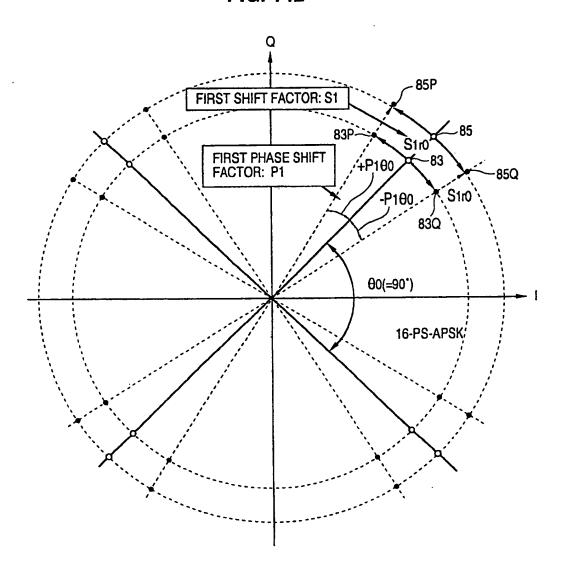
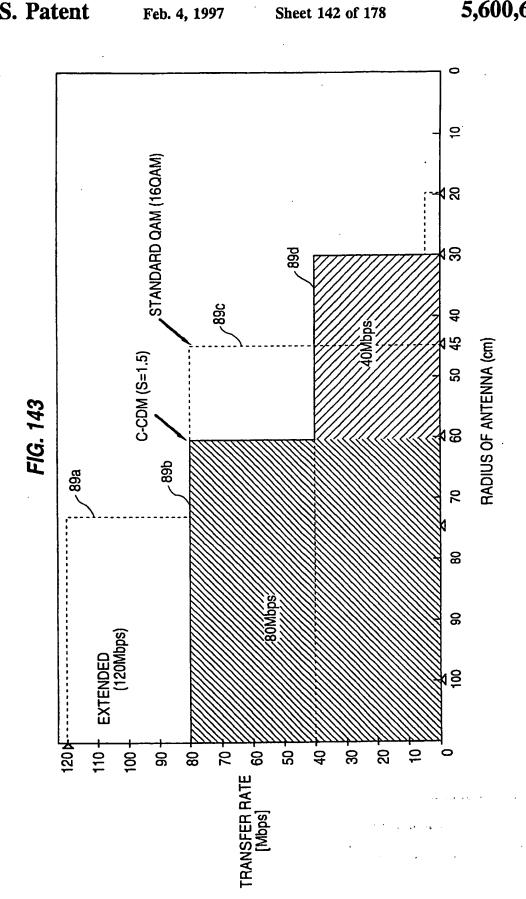


FIG. 142





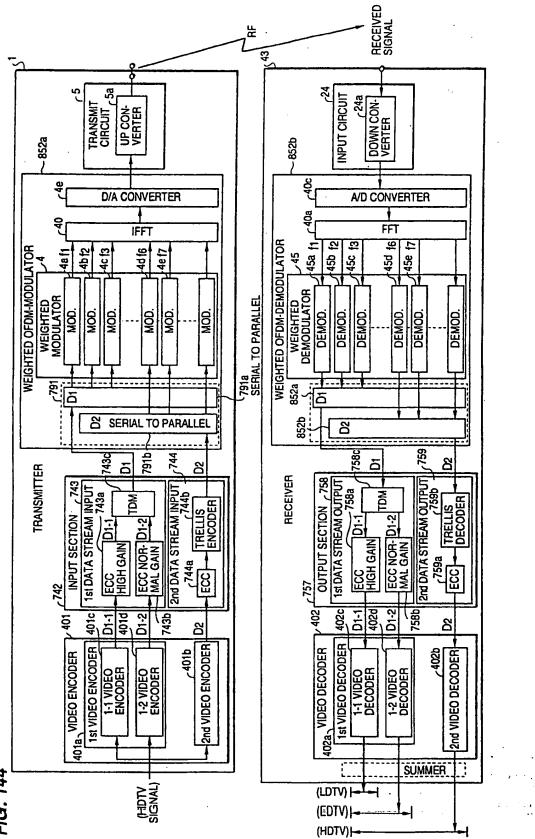


FIG. 14

FIG. 145(a)

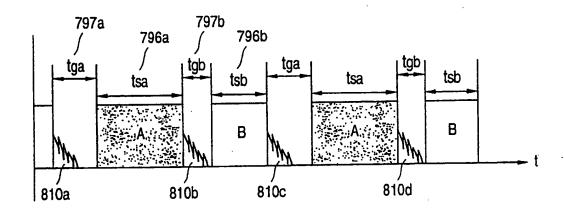
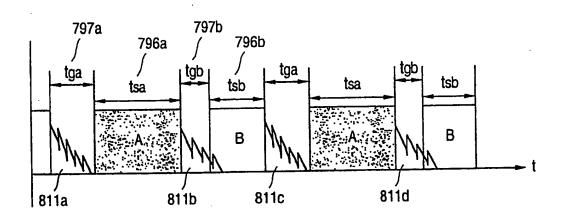
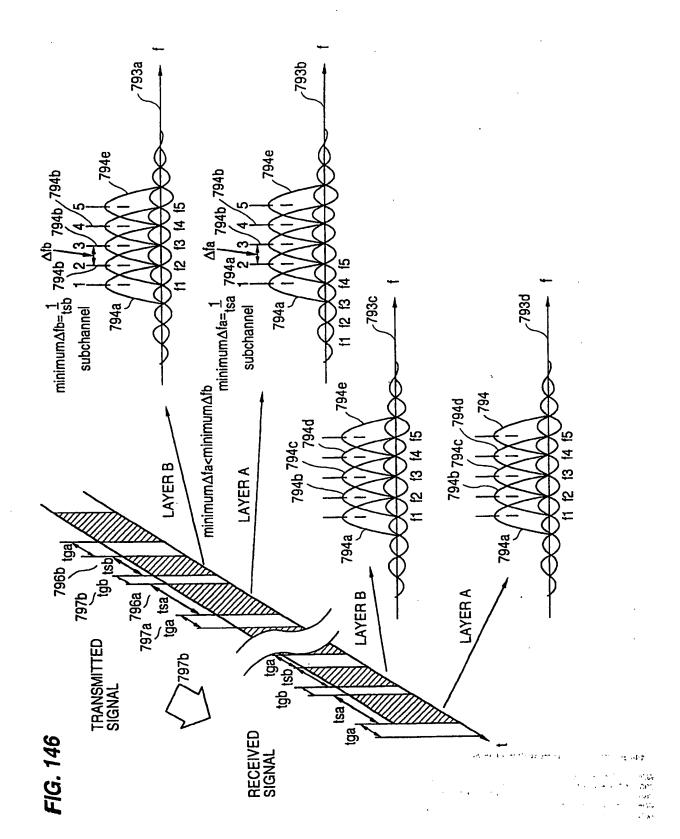
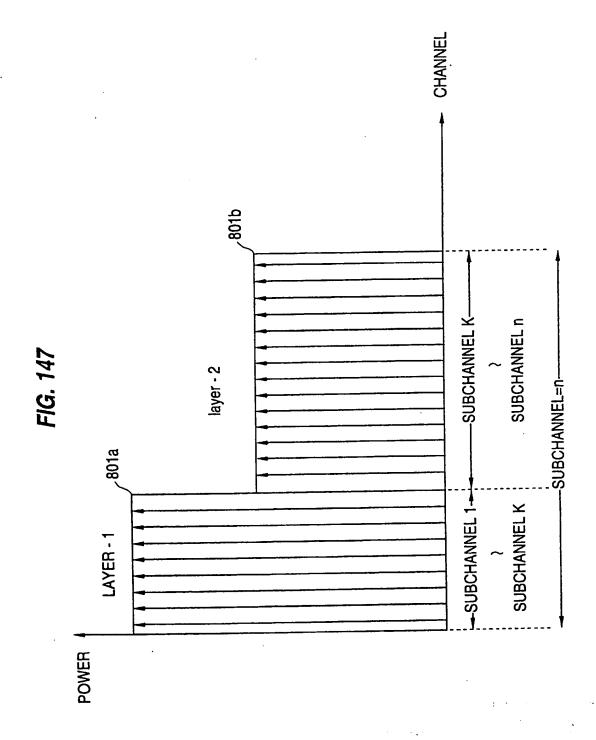


FIG. 145(b)





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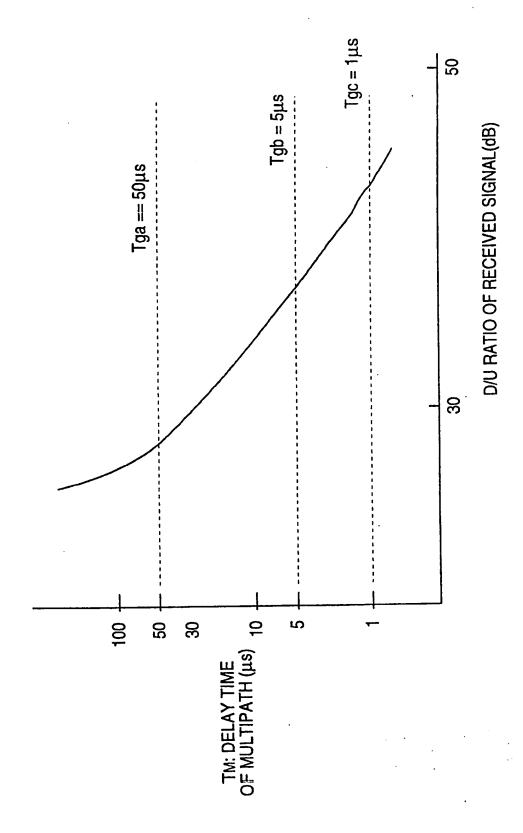
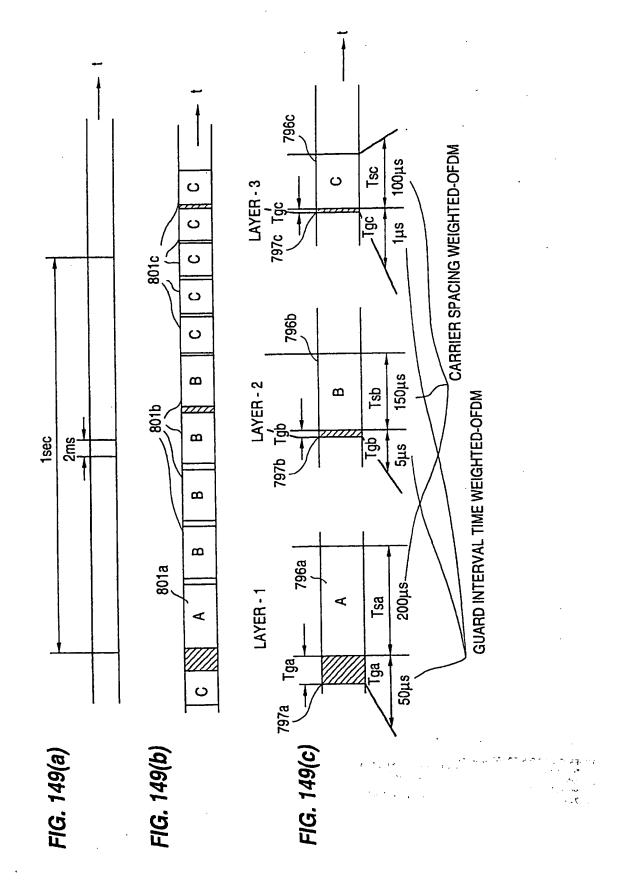
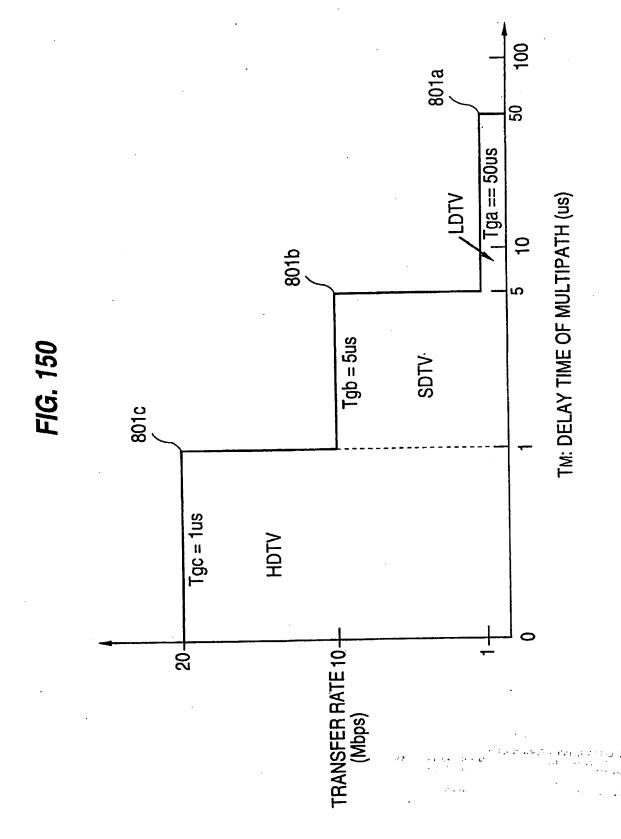
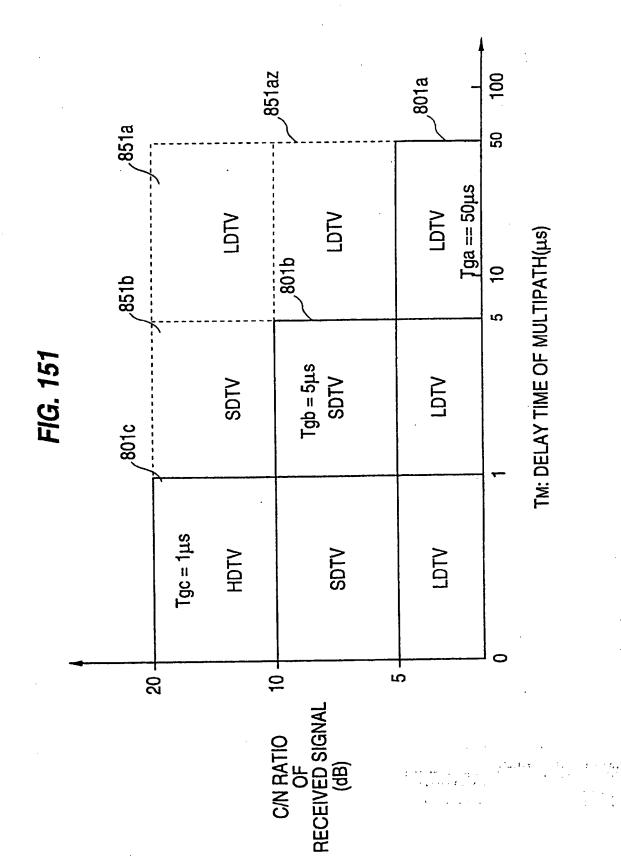


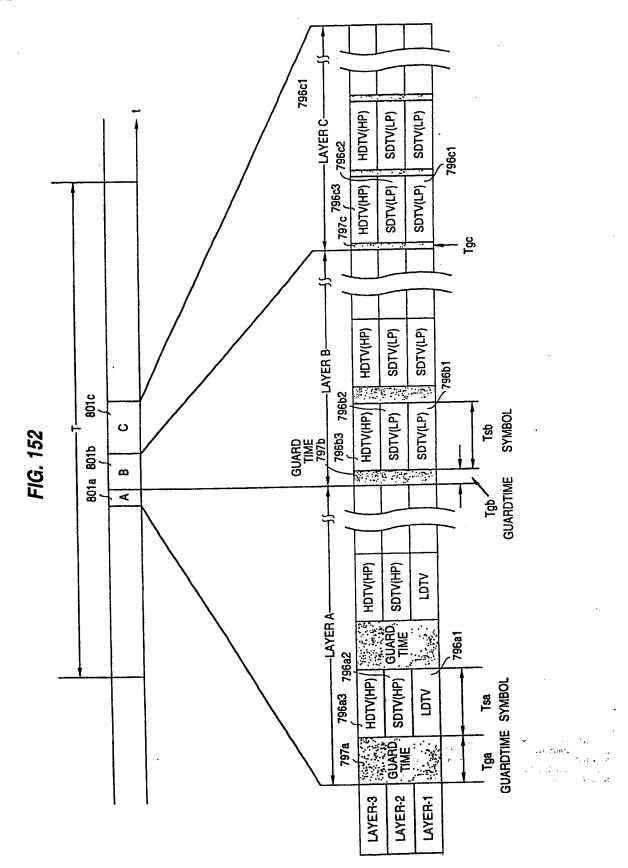
FIG. 148

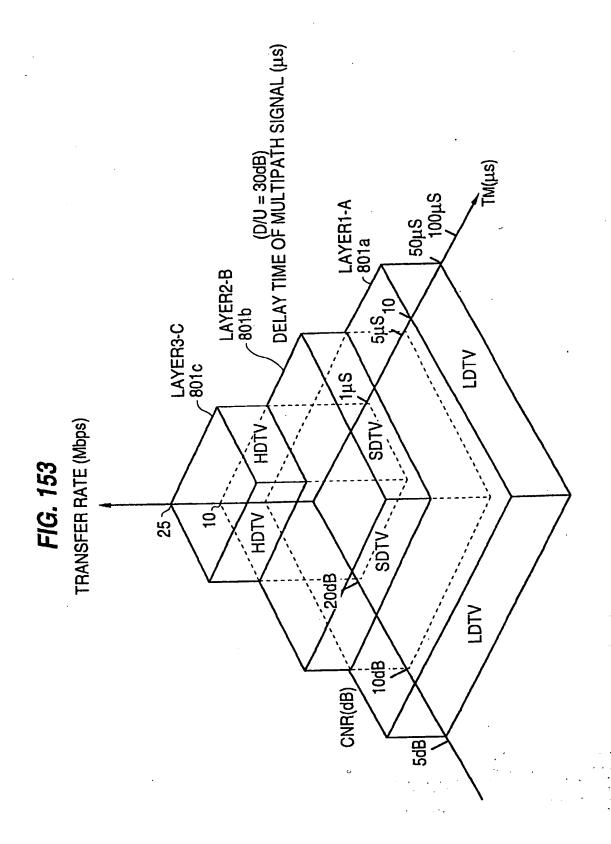


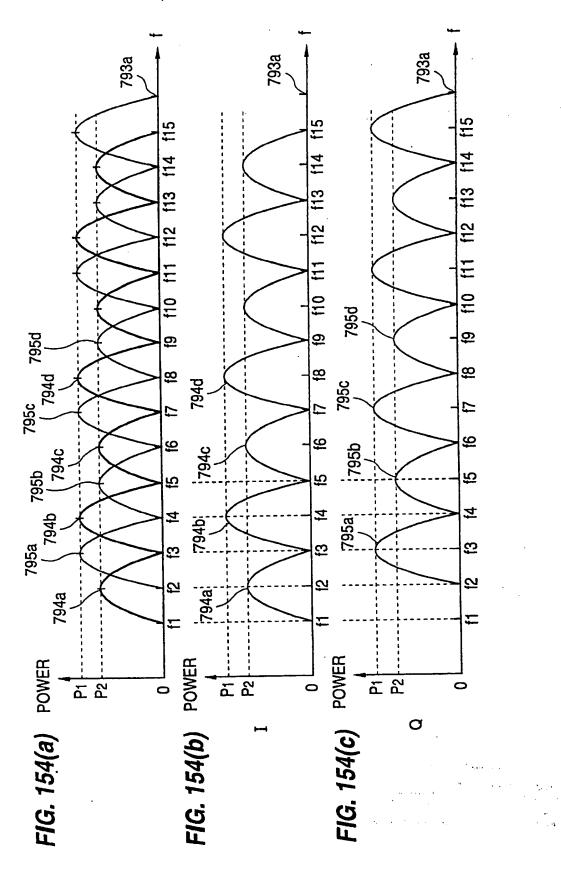
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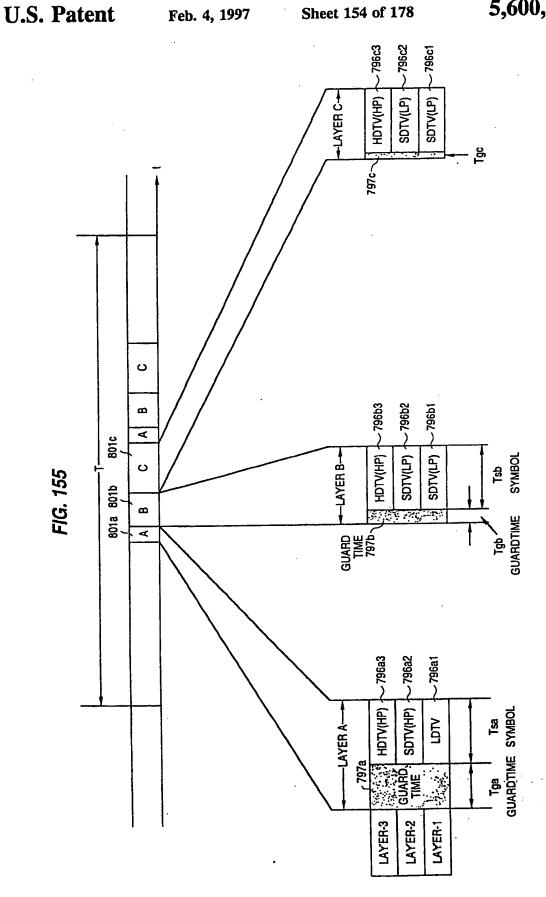












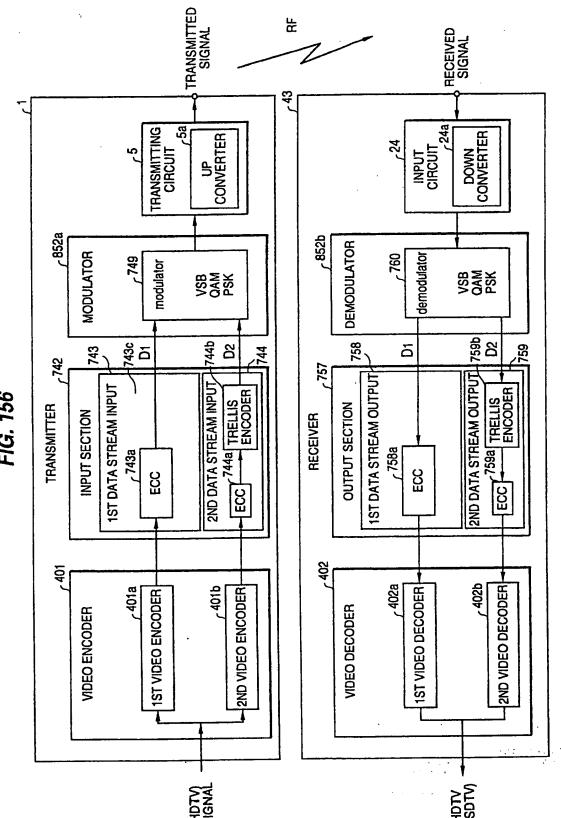
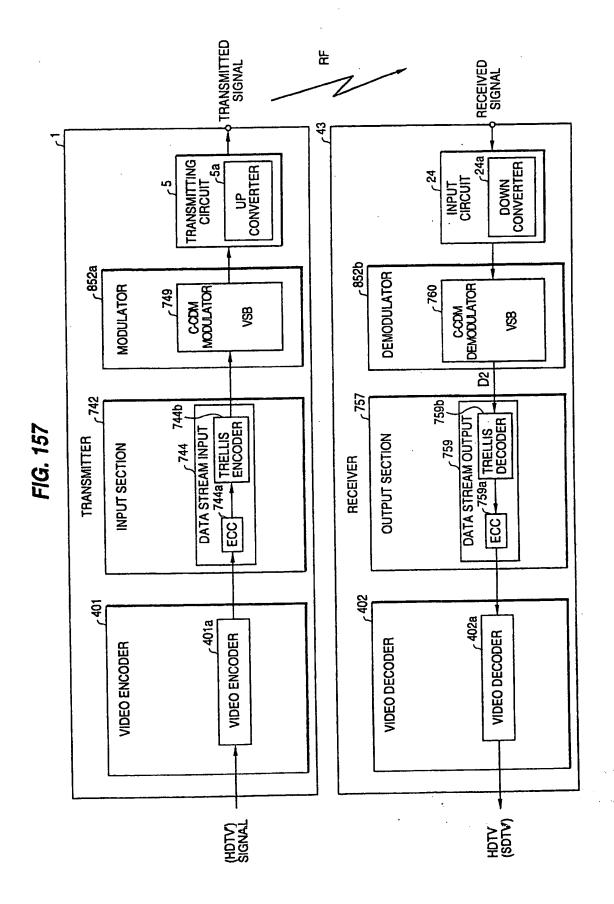
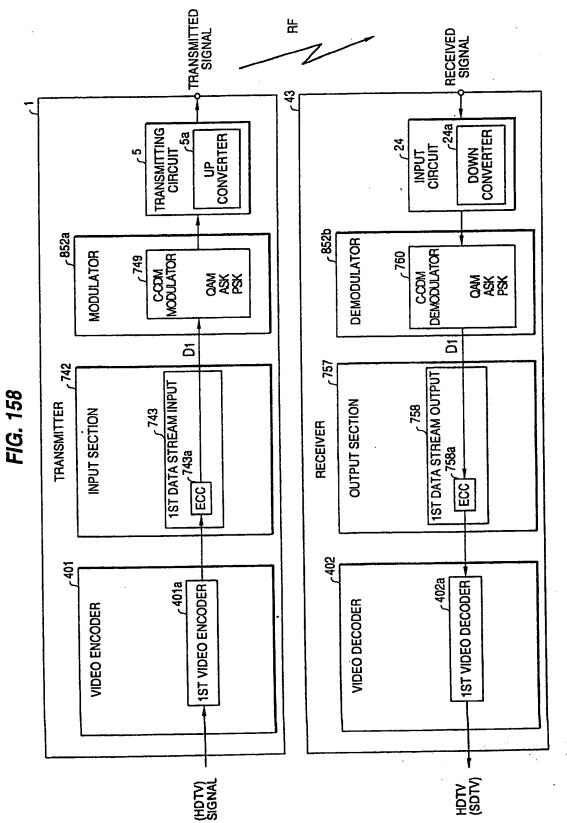
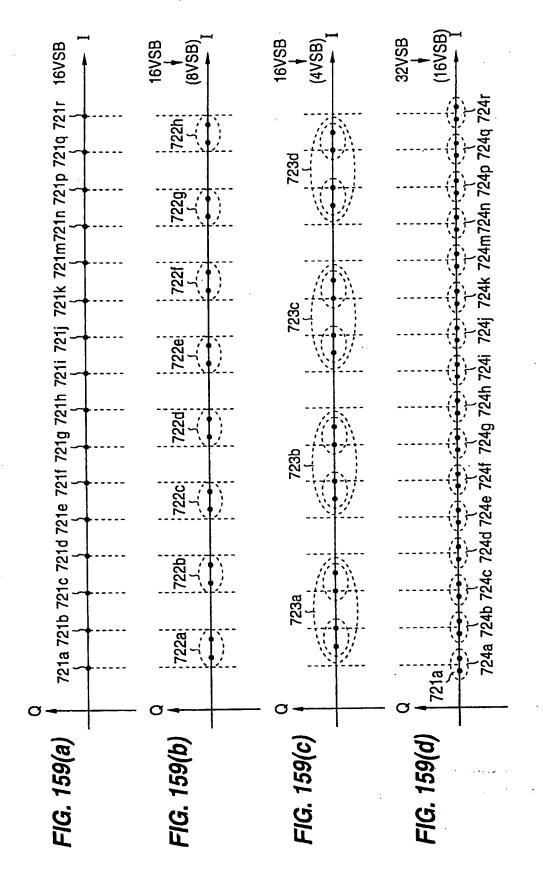


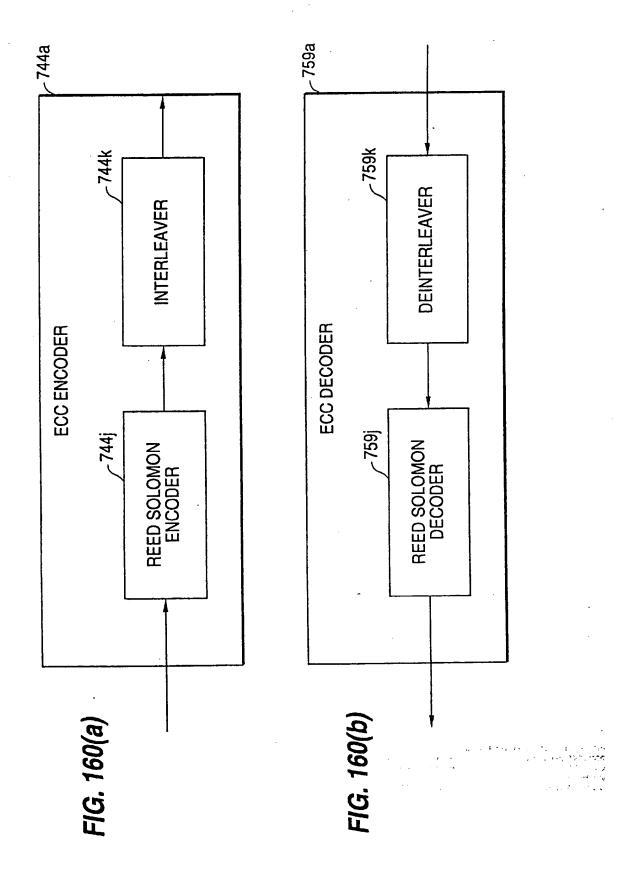
FIG. 156

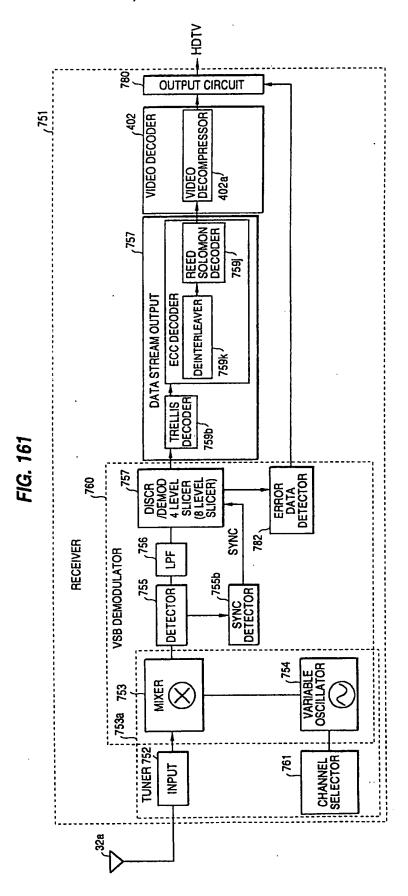




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VSB SIGNAL

4VSB 8VSB 16VSB

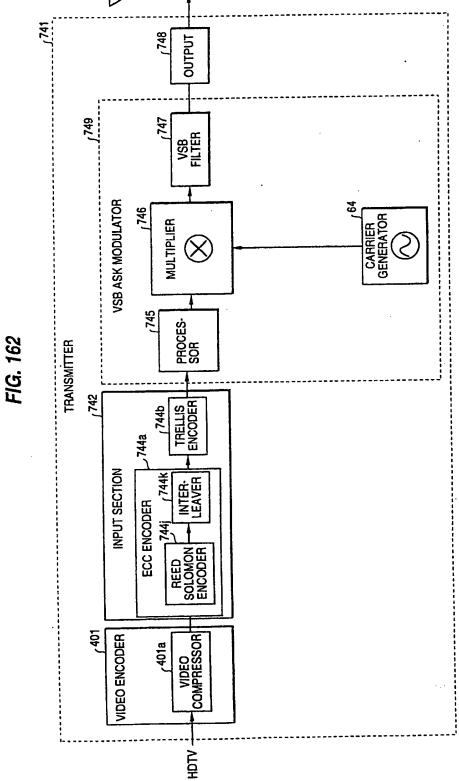


FIG. 163

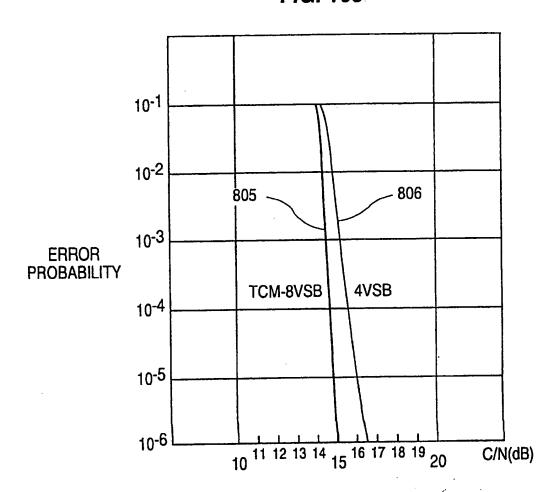
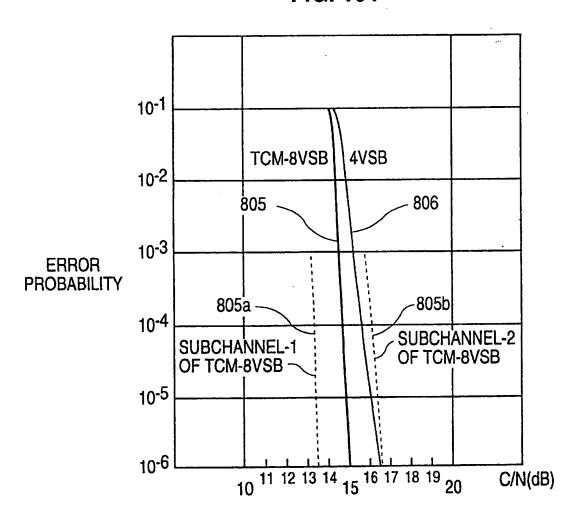


FIG. 164



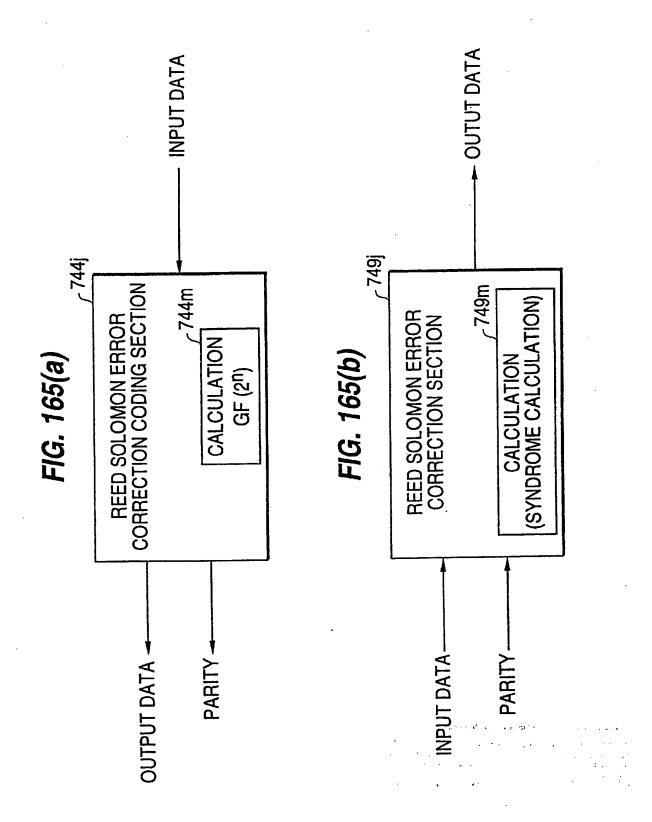
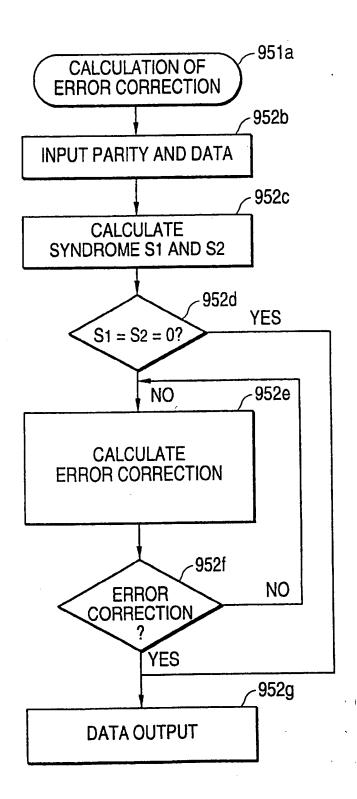
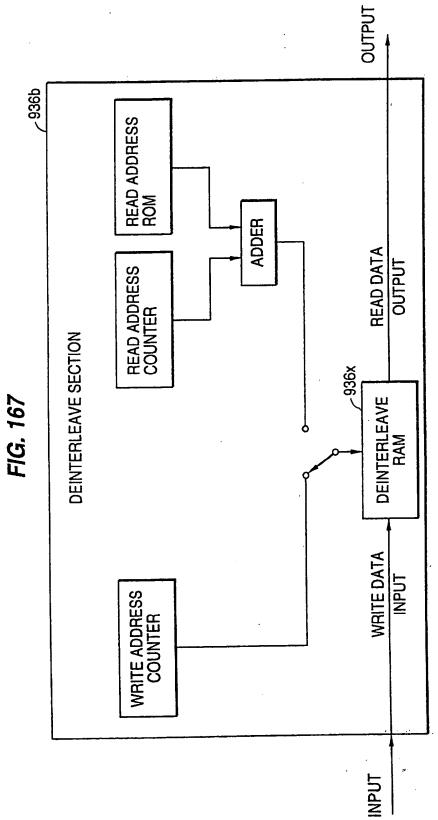
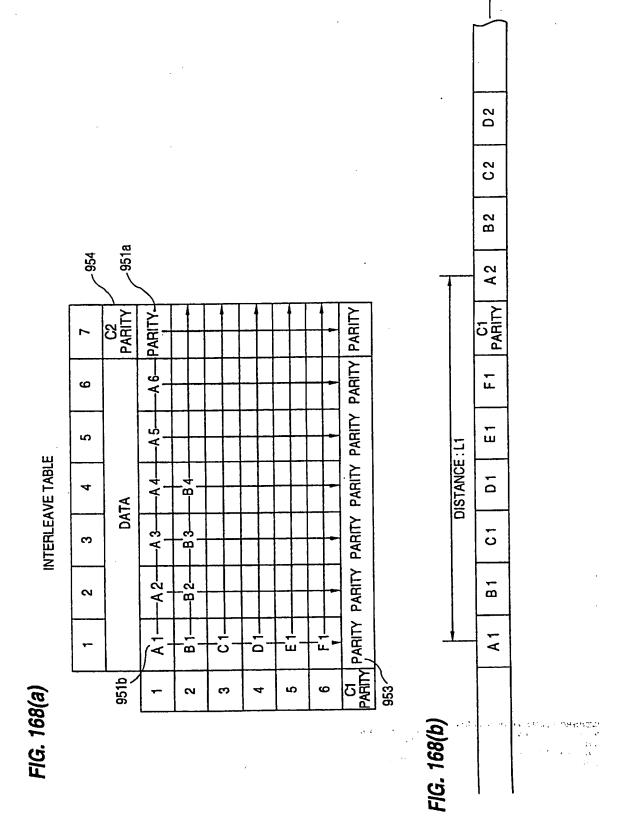


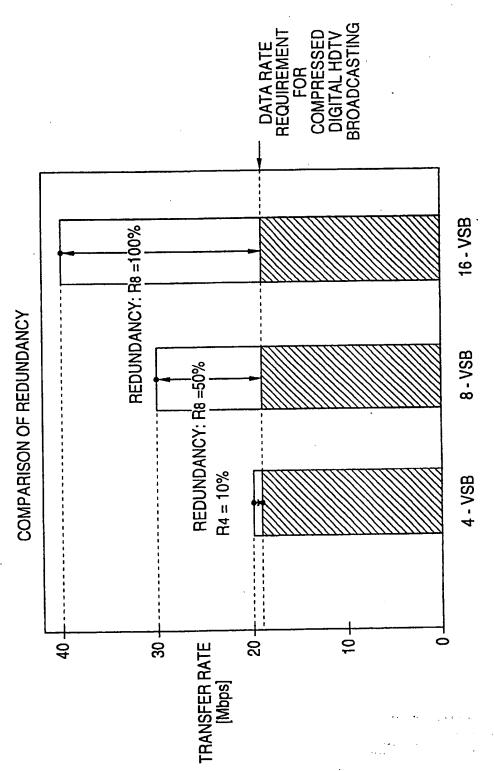
FIG. 166











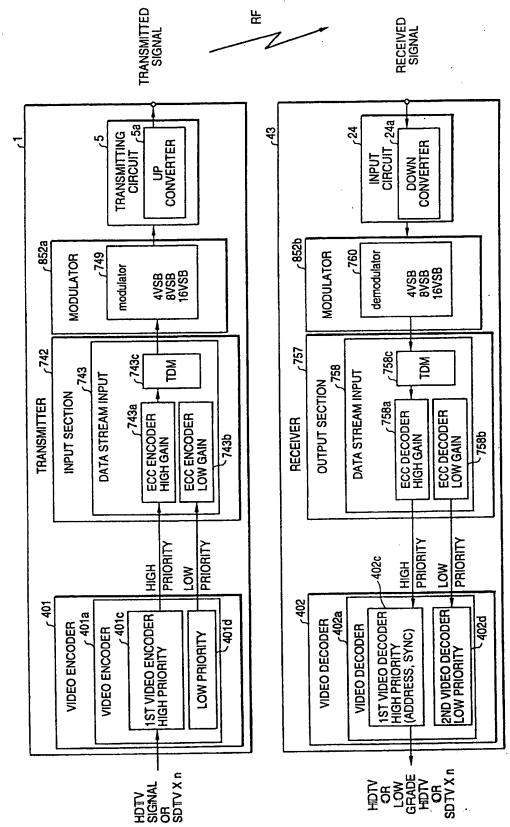
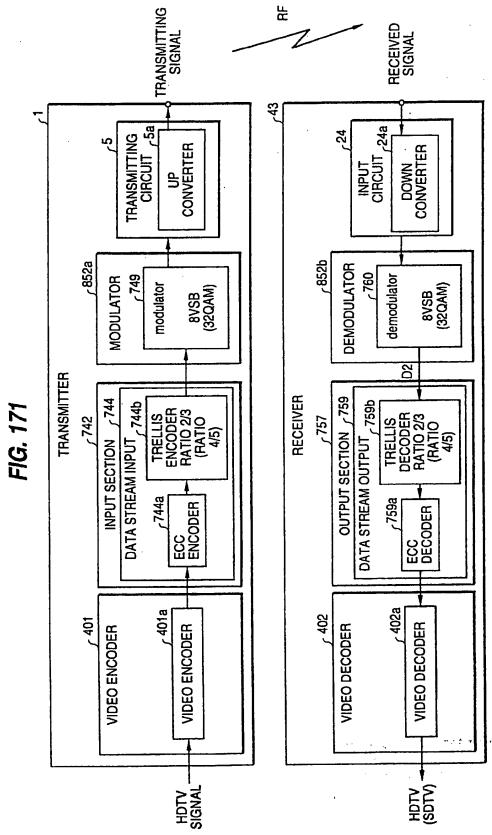


FIG. 170



H

TRANSMITTED SIGNAL RECEIVED SIGNAL INPUT CIRCUIT _f 24a TRANSMITTING CIRCUIT , 5a 5 Ý īί UP CONVERTER UP CONVERTER 852b DEMODULATOR 749 demodulator MODULATOR modulator 4VSB 8VSB 16VSB 4VSB 8VSB 16VSB TRELLIS DECODER RATIO 2/3 (RATIO 4/5) TRELLIS ENCODER RATIO 2/3 (RATIO 4/5) 759b 743c 757 DATA STREAM OUTPUT **OUTPUT SECTION** INPUT SECTION DATA STREAM INPUT TRANSMITTER ECC DECODER HIGH GAIN ECC DECODER LOW GAIN ECC ENCODER HIGH GAIN ECC ENCODER LOW GAIN RECEIVER 758b 743b PRIORITY PRIORITY PRIORITY PRIORITY HGH 된 <u>%</u> <u></u>80 4 1ST VIDEO DECODER HIGH PRIORITY (ADDRESS, SYNC) ZND VIDEO DECODER 7 401c VIDEO DECODER 1ST VIDEO ENCODER HIGH PRIORITY 402d 401d VIDEO ENCODER VIDEO DECODER VIDEO ENCODER **LOW PRIORITY** HDTV OR GRADE HDTV OR SDTV Xn (HDTV) SIGNAL

FIG. 172

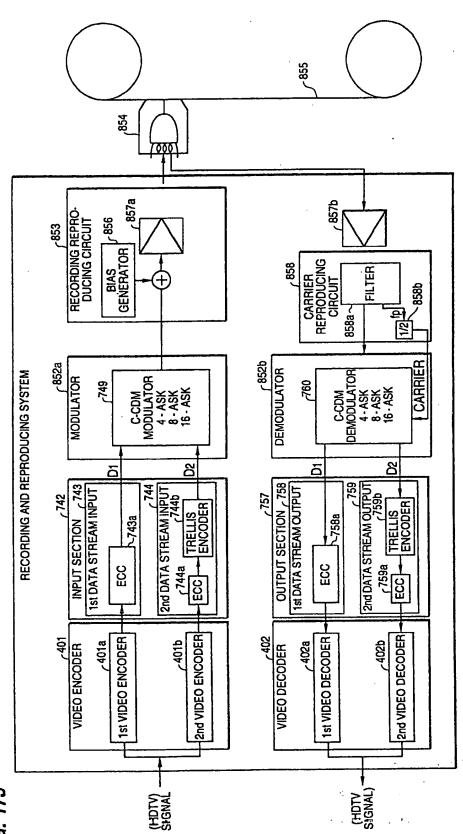
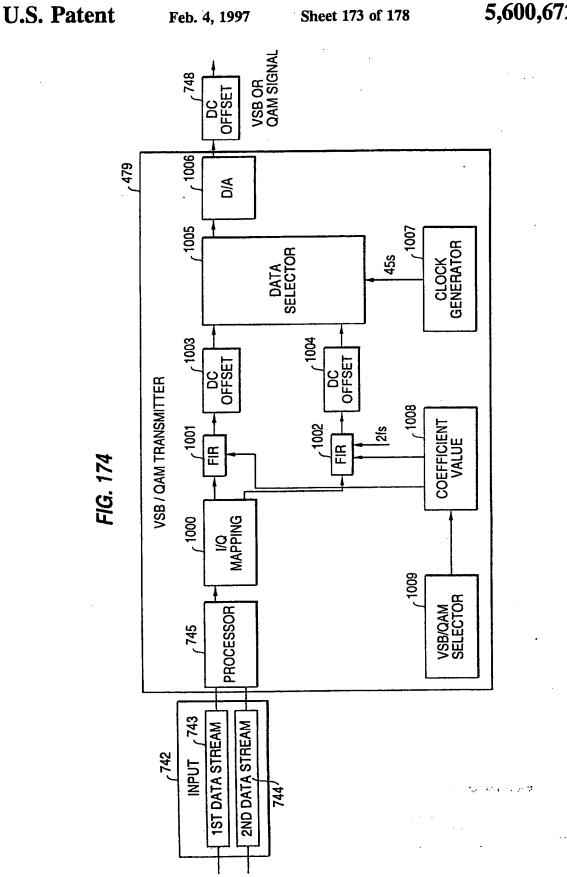
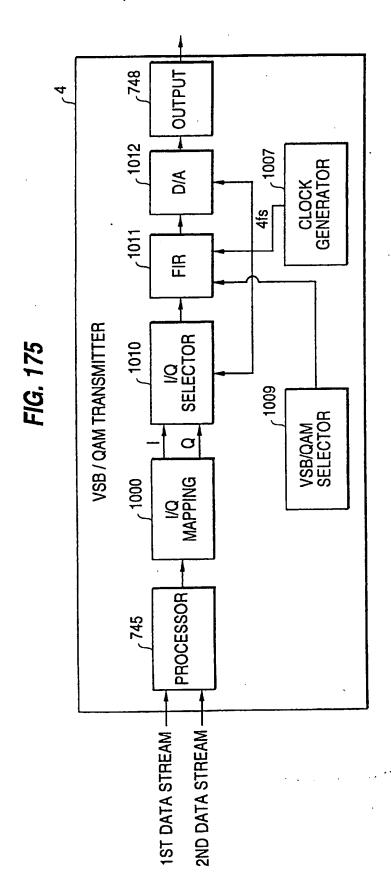
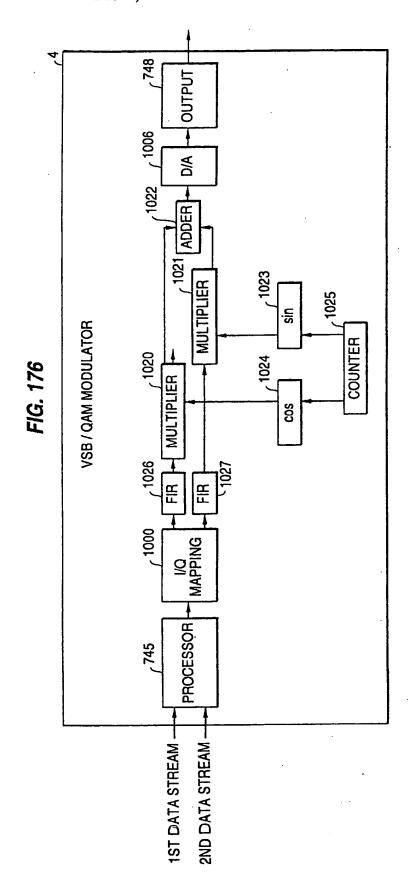


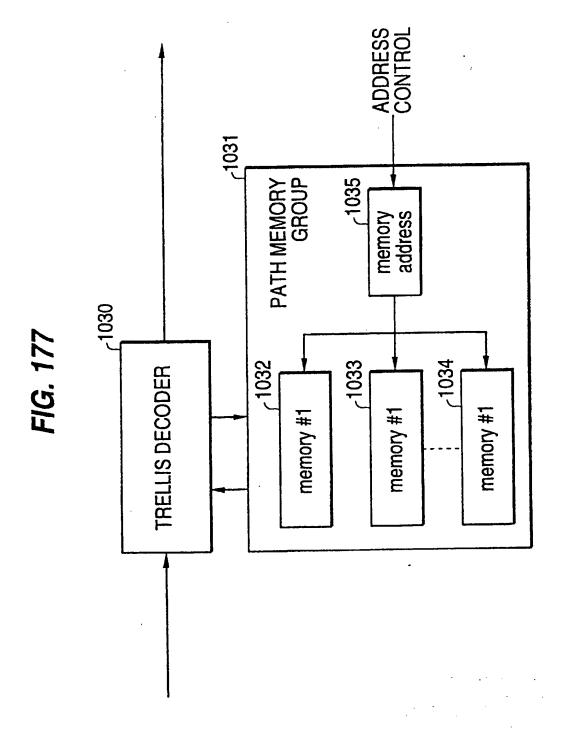
FIG. 173







Feb. 4, 1997



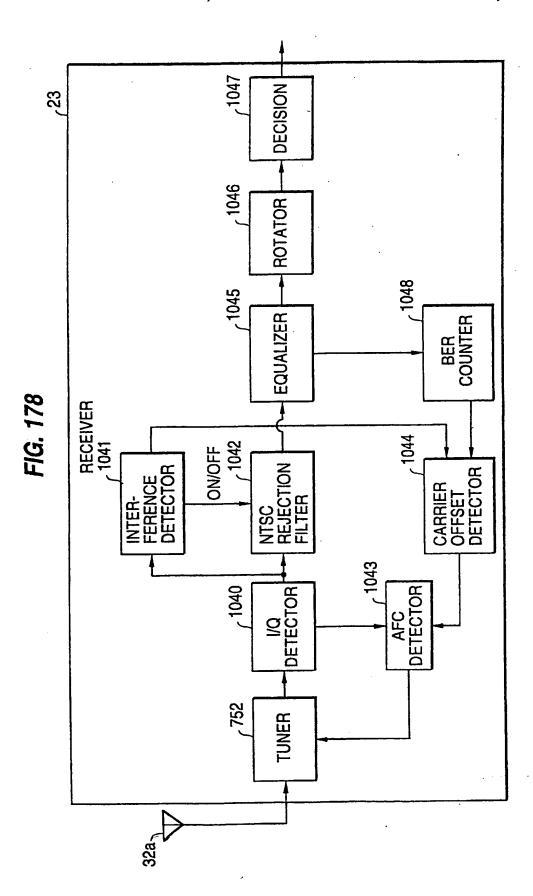


FIG. 179

